

Microlithography: Trends, Challenges, and Potential Solutions

Alfred K. Wong

Department of Electrical and Electronic Engineering
The University of Hong Kong, Pokfulam Road, Hong Kong
awong@eee.hku.hk

Anthony Yen and Walt Trybula

International Sematech
2706 Montopolis Drive, Austin, TX 78741, USA

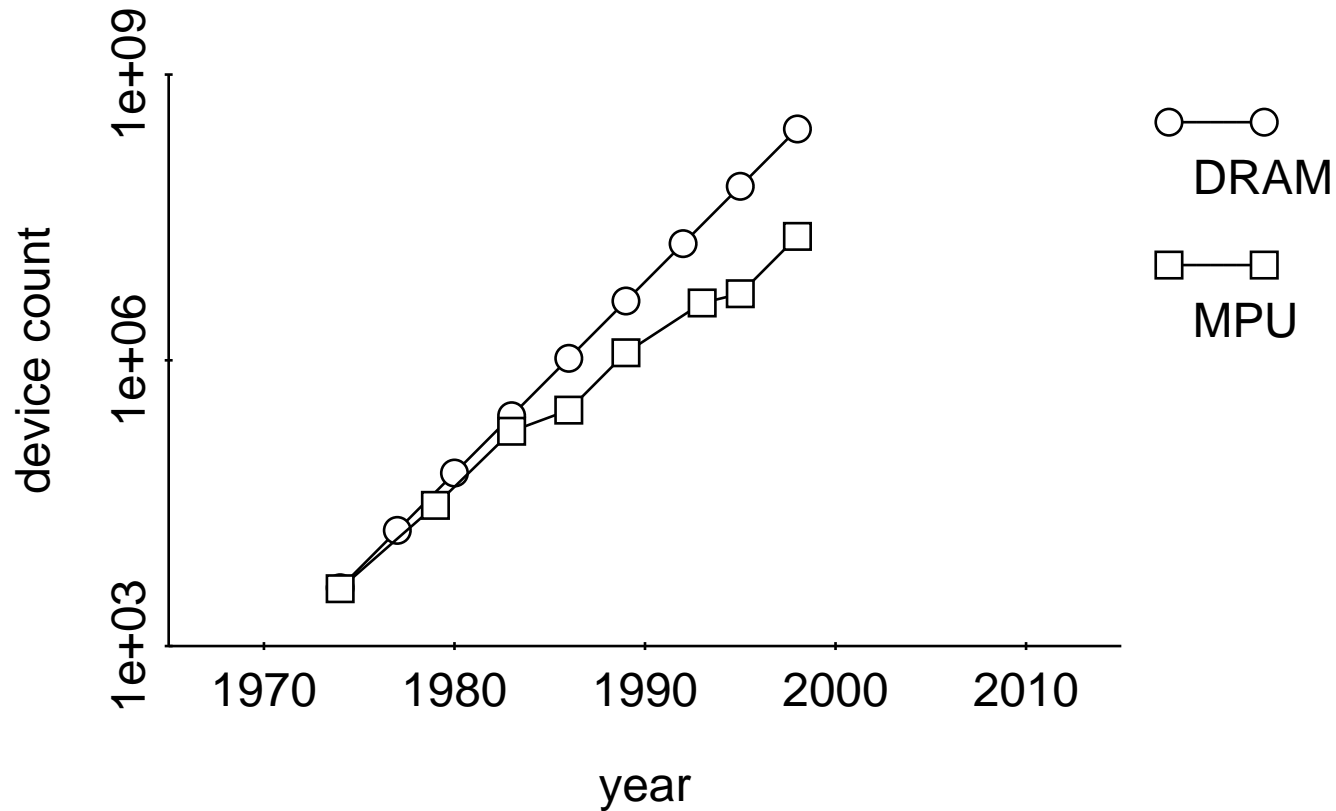
August 18, 2002

Outline

- Moore's law and microlithography
 - introduction
 - factors affecting resolution
 - trends
- low- k_1 challenges
 - resolution limit
 - image distortion and degradation
 - design and cost implications
- potential solutions

Moore's law

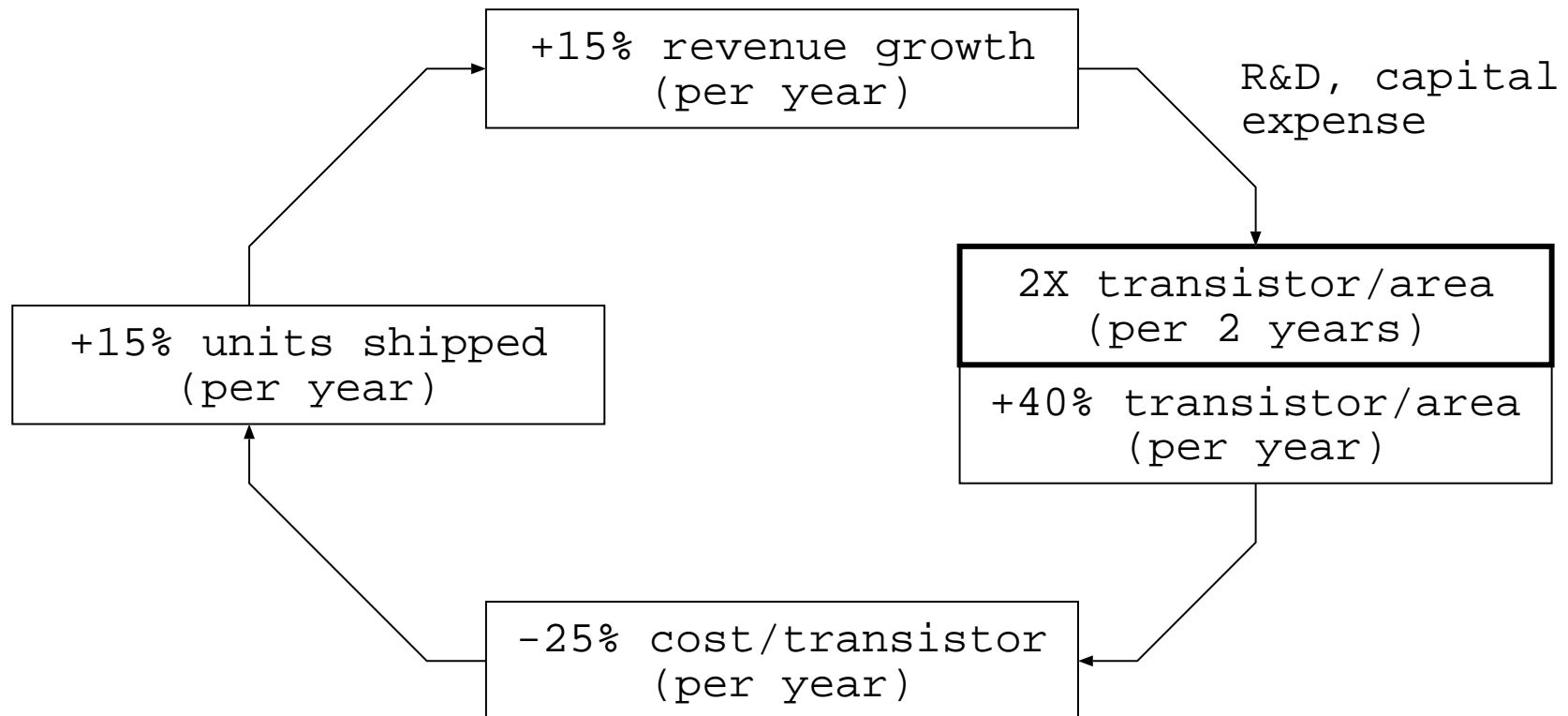
transistor count per chip increases exponentially with time



'The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that, when plotted on semi-log paper, approximates a straight line.'—Gordon Moore (1995).

Simplified semiconductor cycle

assuming constant chip price



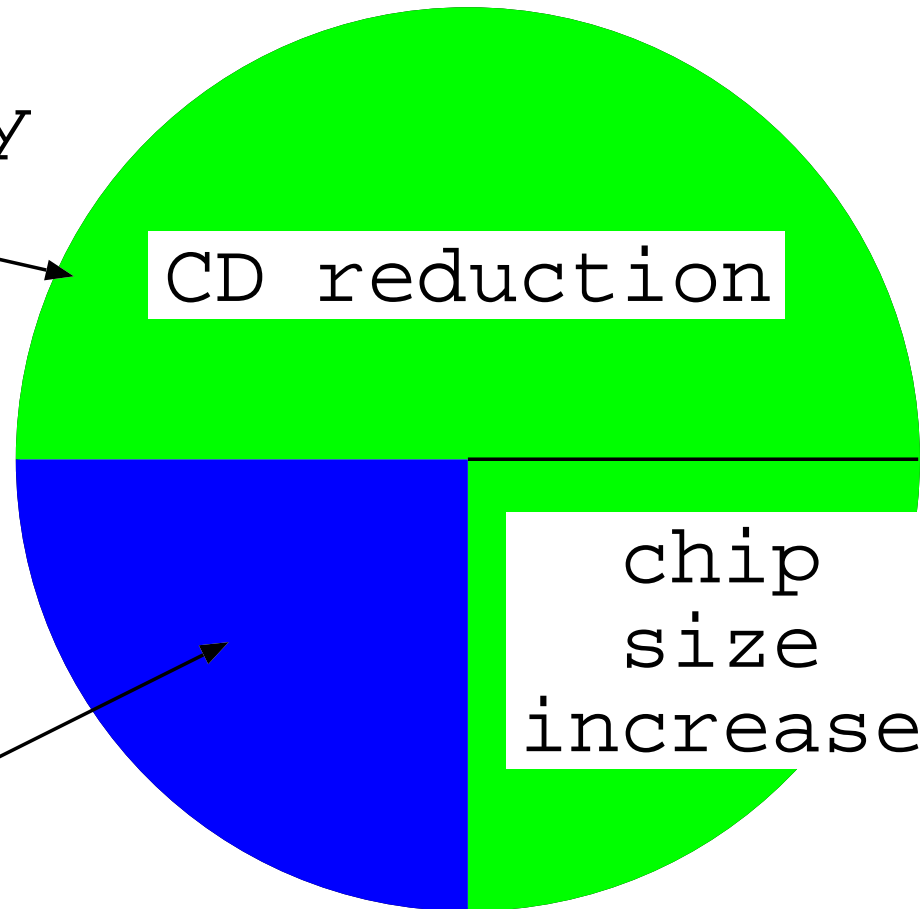
Contributors to transistor count increase

photolithography

CD reduction

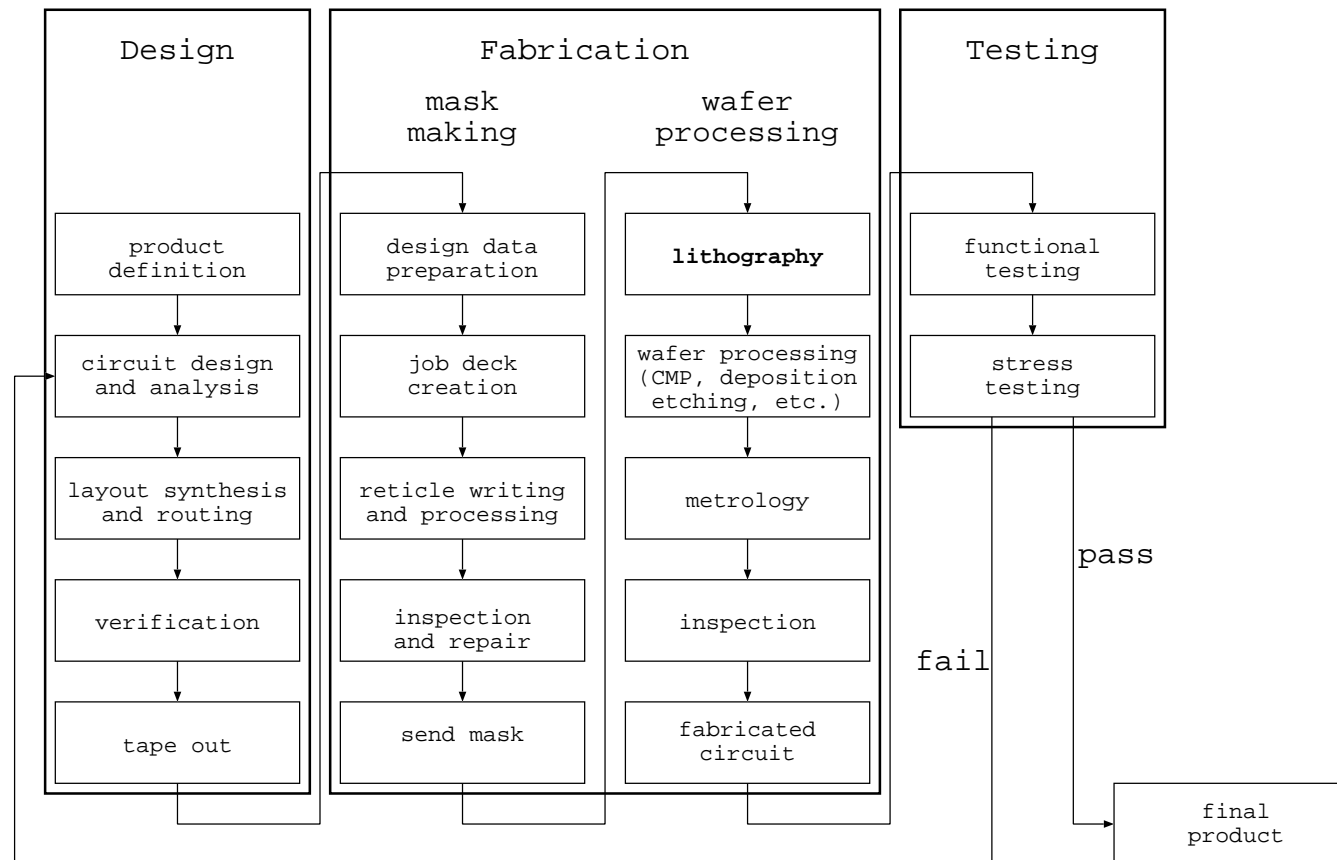
design
innovation

chip
size
increase

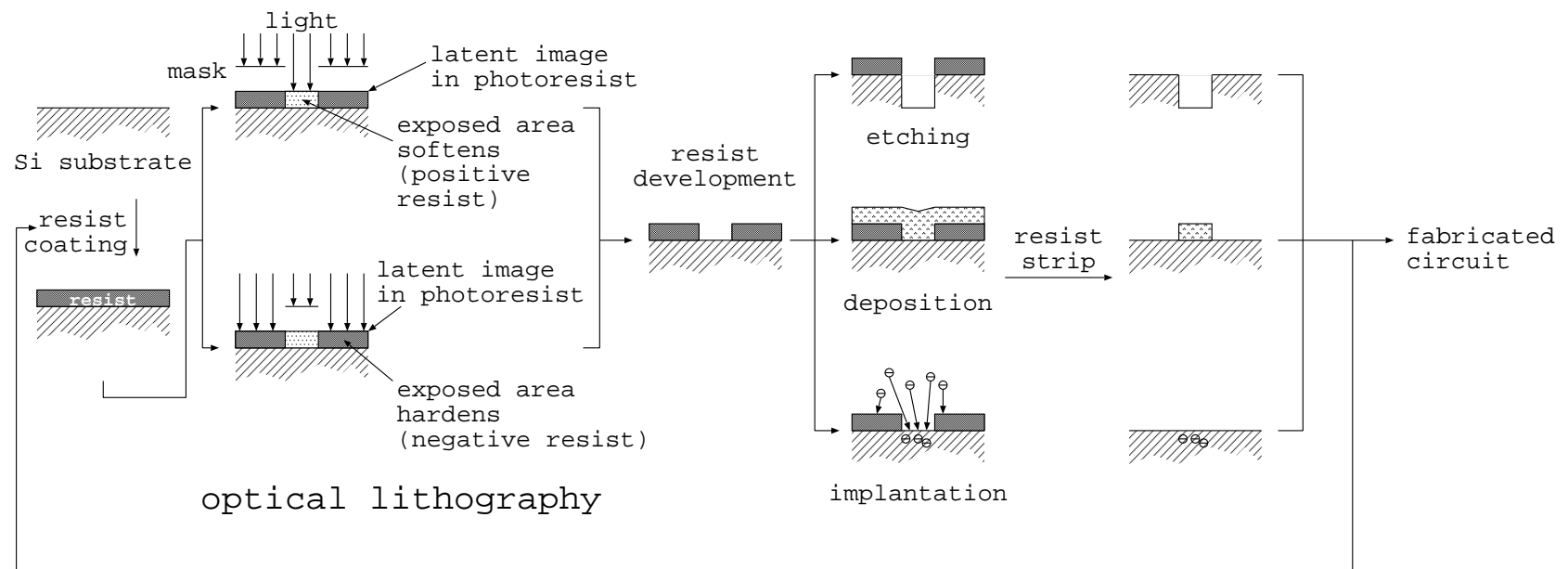


Integrated circuit creation process

a fabrication-centric view



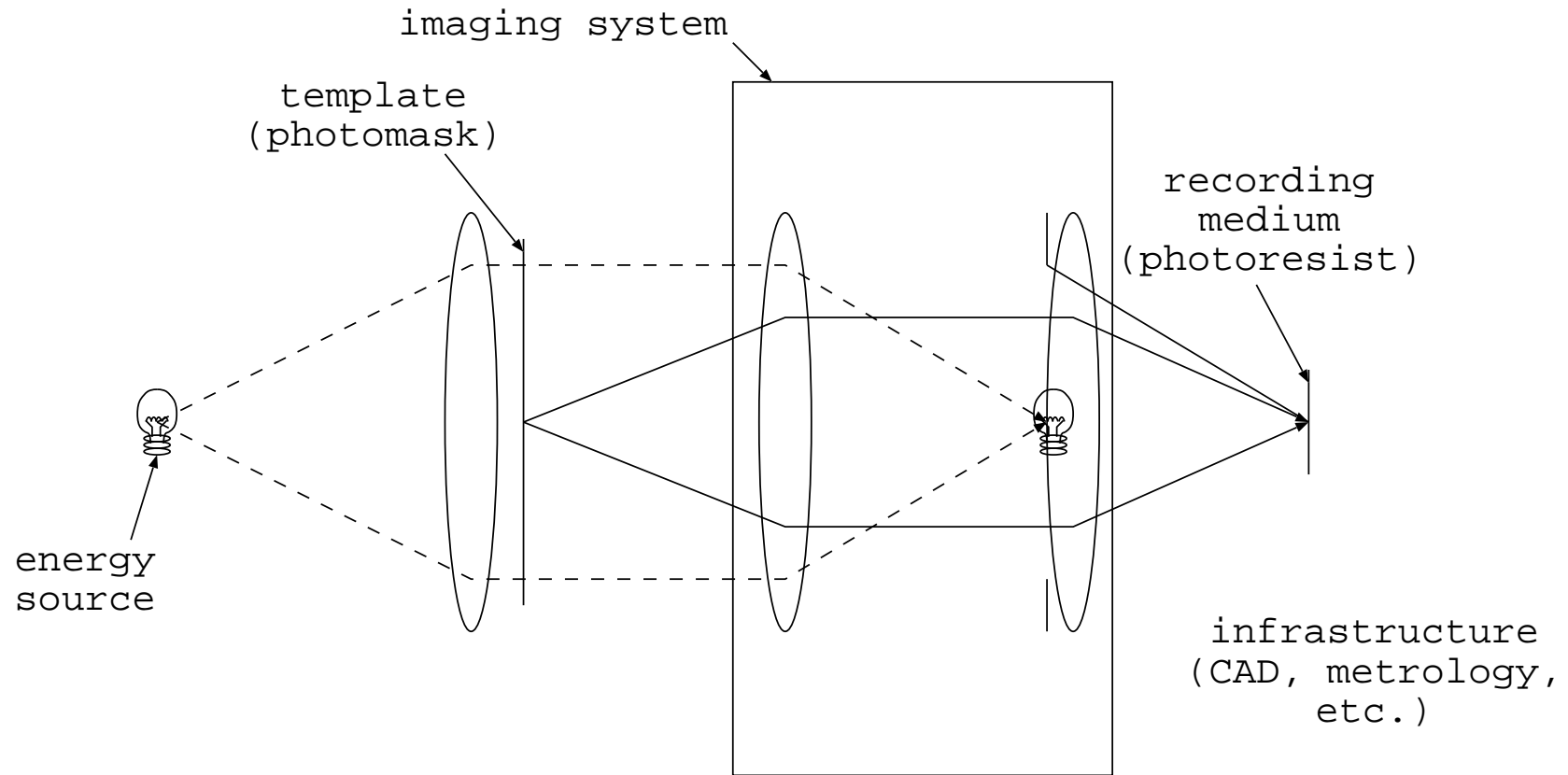
IC fabrication process



Requirements of microlithography

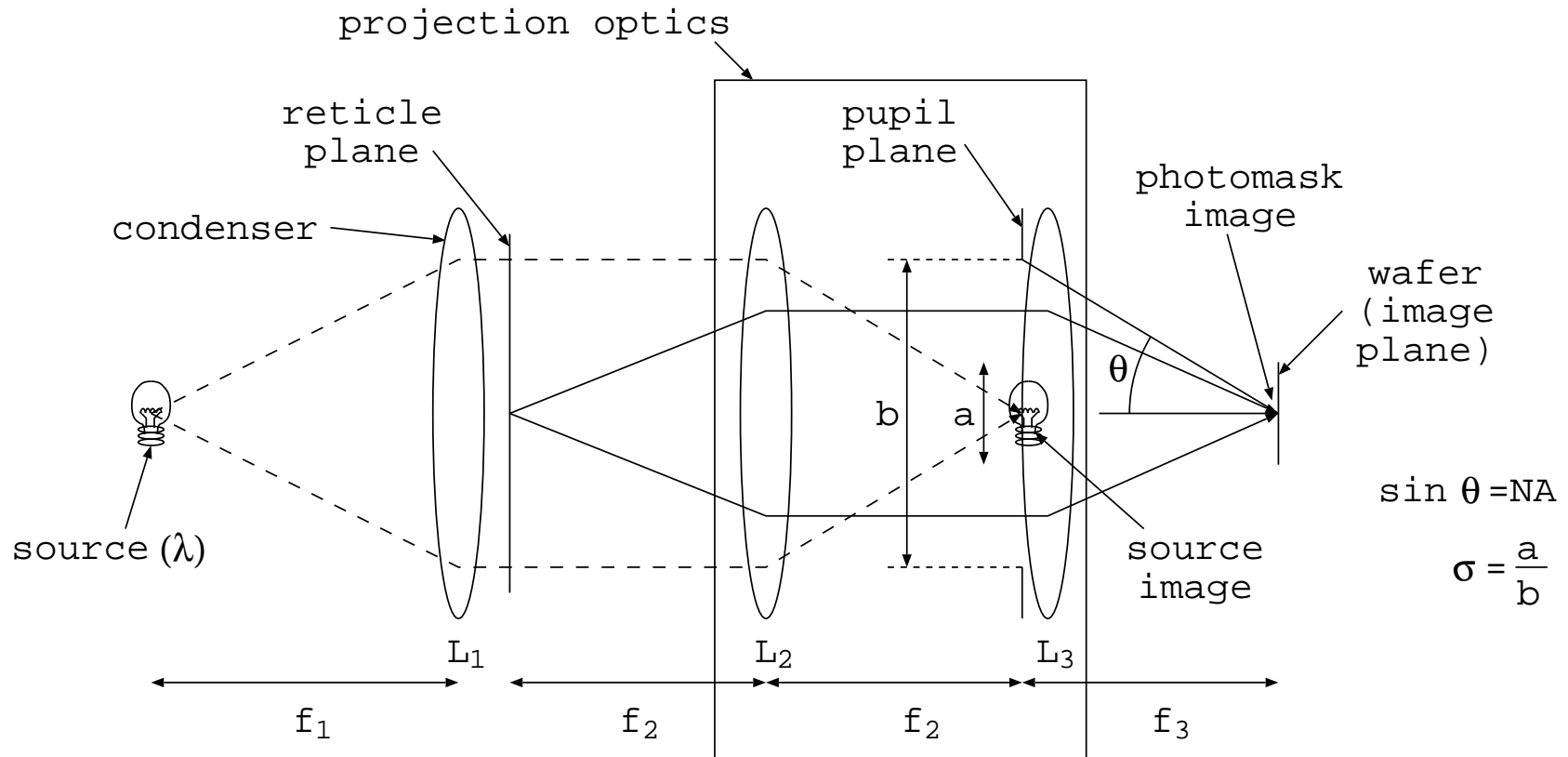
- imaging capabilities
 - ☐ resolution
 - ☐ large field size
- process control
 - ☐ linewidth tolerance
 - ☐ placement control
- materials
 - ☐ bright light source
 - ☐ practical lens and template materials
 - ☐ resolution and robustness of recording medium
- infrastructure
 - ☐ metrology
 - ☐ CAD
 - ☐ mechanics
- low cost of ownership

Basic components of optical lithography



Refined optical system

still much simplified



Three parameters affecting resolution

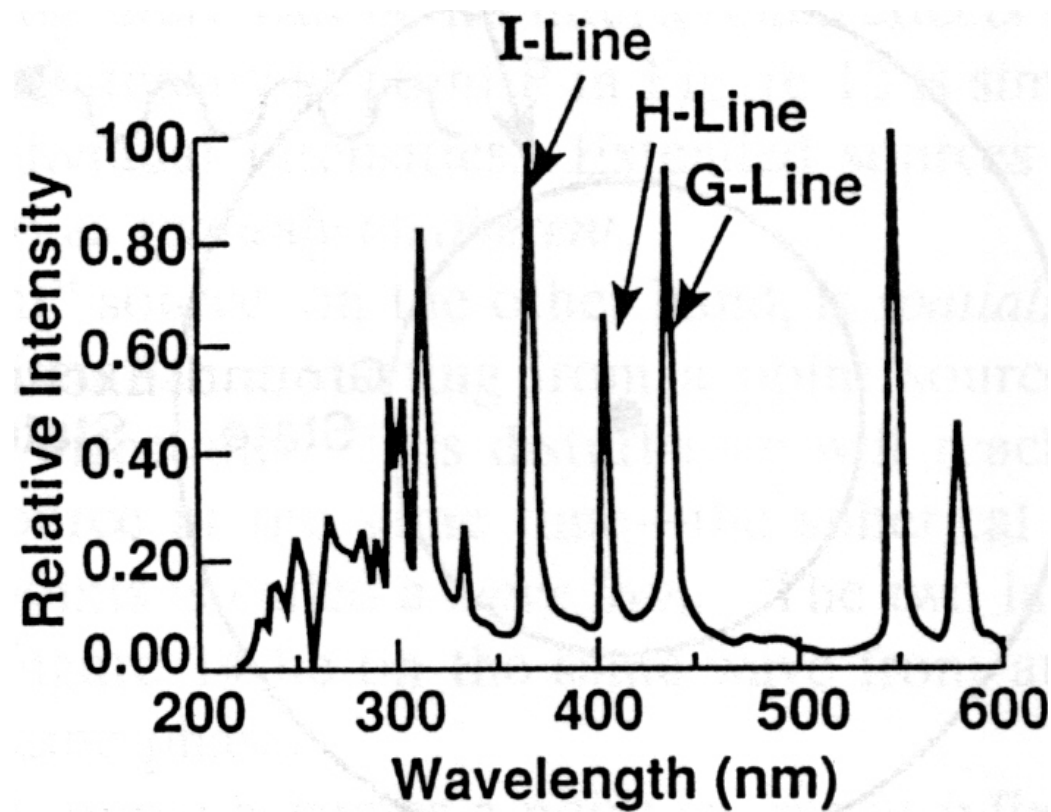
$$\text{CD} = k_1 \times \frac{\lambda}{\text{NA}}$$

need to work on all three

Issues with wavelength changes

- availability of light source
 - ☐ energetic
 - ☐ reliable
- oxygen-free environment < 193 nm (e. g., 157 nm)
- new optical and reticle materials
 - ☐ borosilicate glass
 - ☐ fused silica
 - ☐ modified fused silica (fluorine-doped)
 - ☐ CaF_2 , BaF_2
- new processing materials
 - ☐ resist
 - ☐ ARC
- process integration

Mercury arc discharge



higher NA \longrightarrow narrower spectrum \longrightarrow more spectral power

figure courtesy of Murrae Bowden at Arch Chemicals

Wavelengths for optical lithography

Wavelength (nm)	Light source	Year of introduction	% decrease
436	mercury arc g-line	1970s	—
365	mercury arc i-line	1984	16
248	KrF laser	1989	32
193	ArF laser	1999	23
157	F ₂ laser	>2003	19
126	Ar ₂	unknown	20

- limited by nature (not arbitrary)
- not many more choices

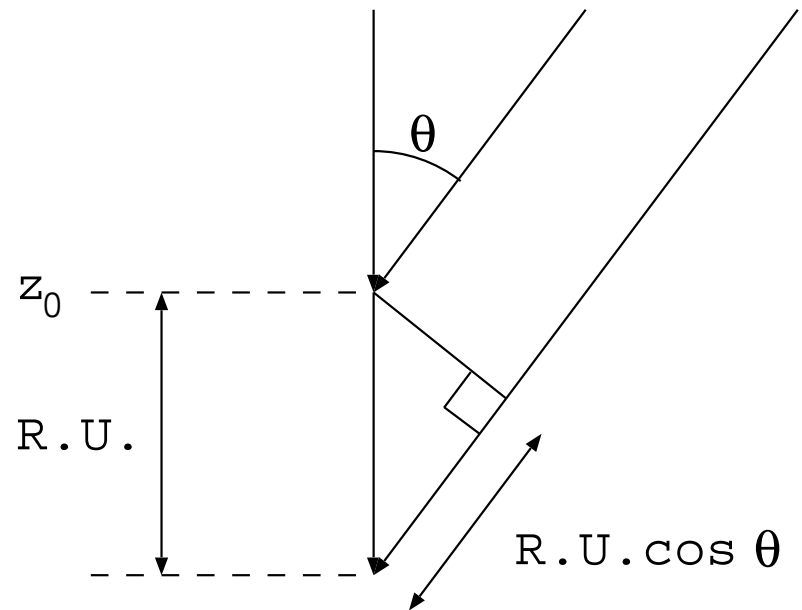
Issues with numerical aperture increase

- physical limit is $\text{NA} = 1$ (in air)
- practical limit ≈ 0.95
 - ☐ physical size of optics
 - ☐ field size
 - ☐ aberration control
 - ☐ depth-of-focus
 - ☐ polarization effects

Depth-of-focus dependence

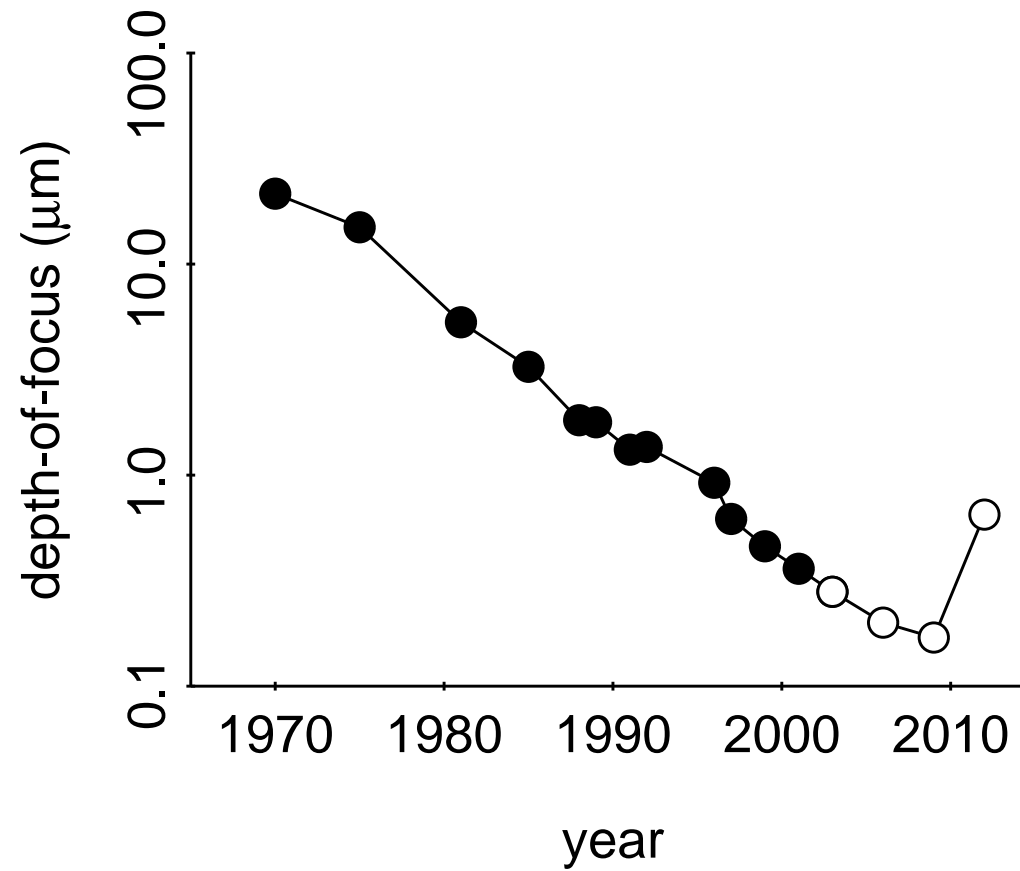
Rayleigh's unit

$$\begin{aligned}\frac{\lambda}{4} &= \text{R. U.} (1 - \cos \theta) \\ \text{R. U.} &= \frac{\lambda}{8 \sin^2(\theta/2)} \\ &= \frac{\lambda}{4 \text{NA}^2} (1 + \sqrt{1 - \text{NA}^2}) \\ &\approx \frac{\lambda}{2 \text{NA}^2} \quad \text{for low-NA} \\ &= \frac{\lambda}{4} \quad \text{as } \text{NA} \rightarrow 1\end{aligned}$$

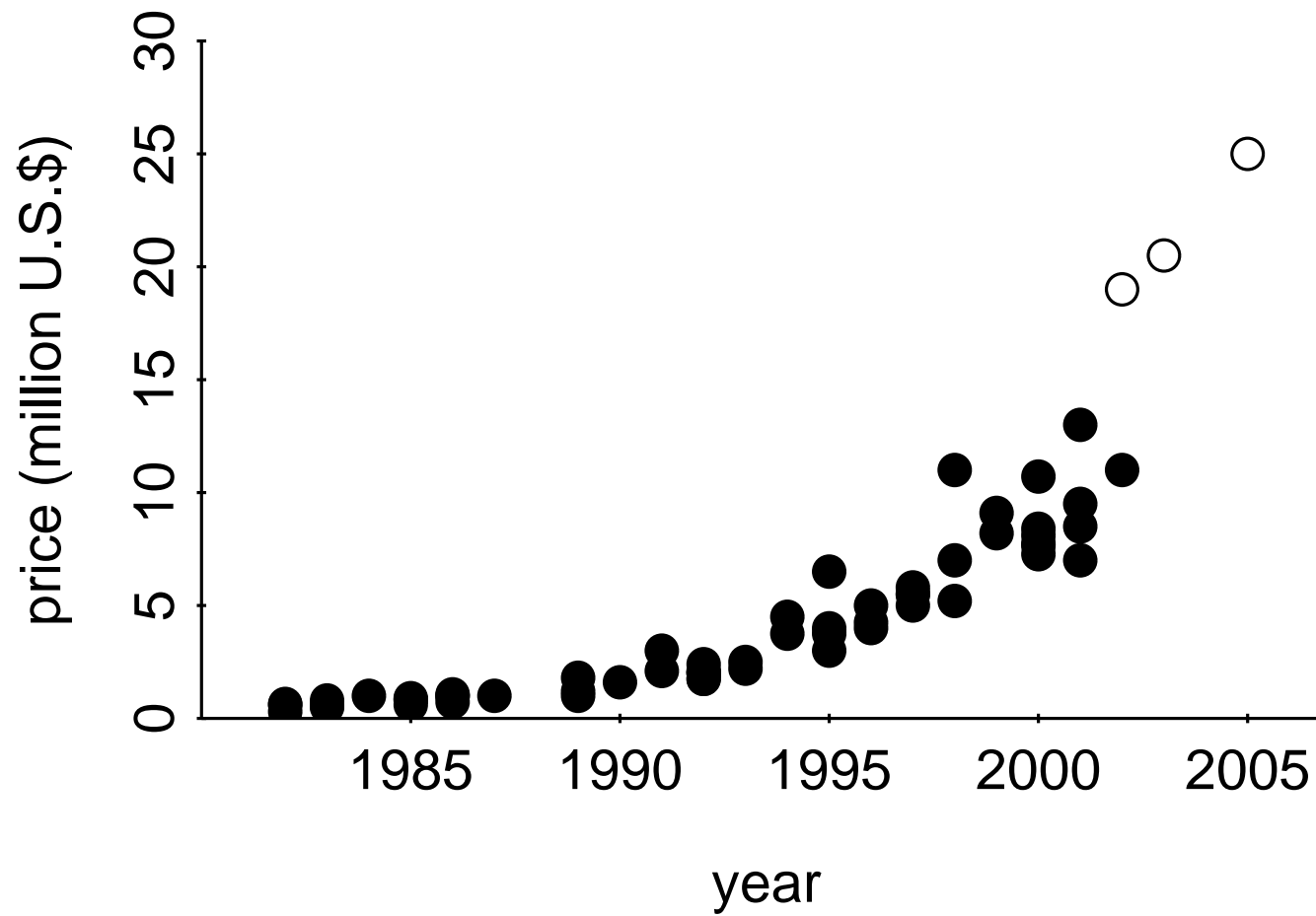


Depth-of-focus trend

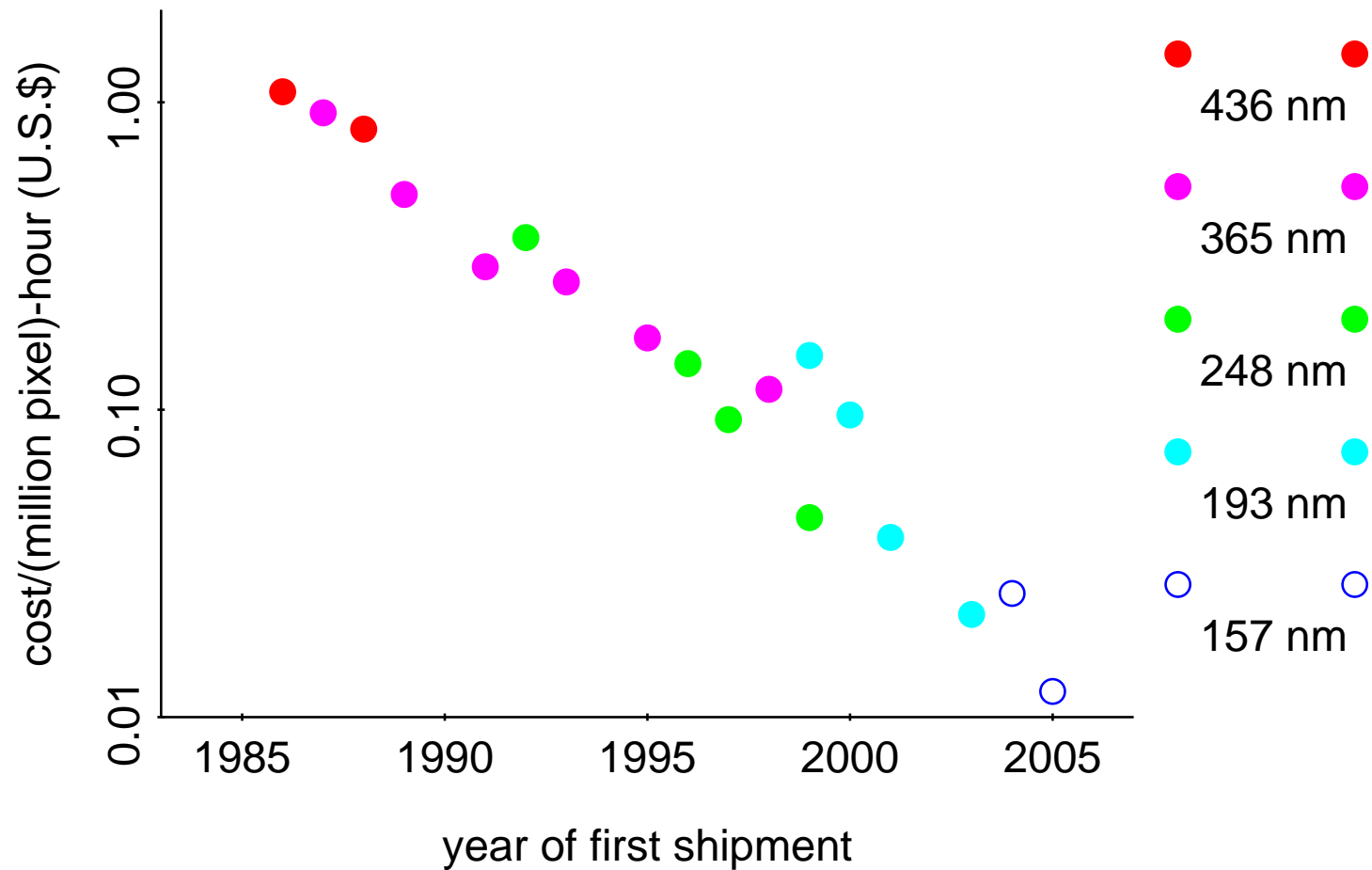
$$2 \times \text{R. U.} = \frac{2\lambda}{4\text{NA}^2} (1 + \sqrt{1 - \text{NA}^2})$$



Cost of exposure system

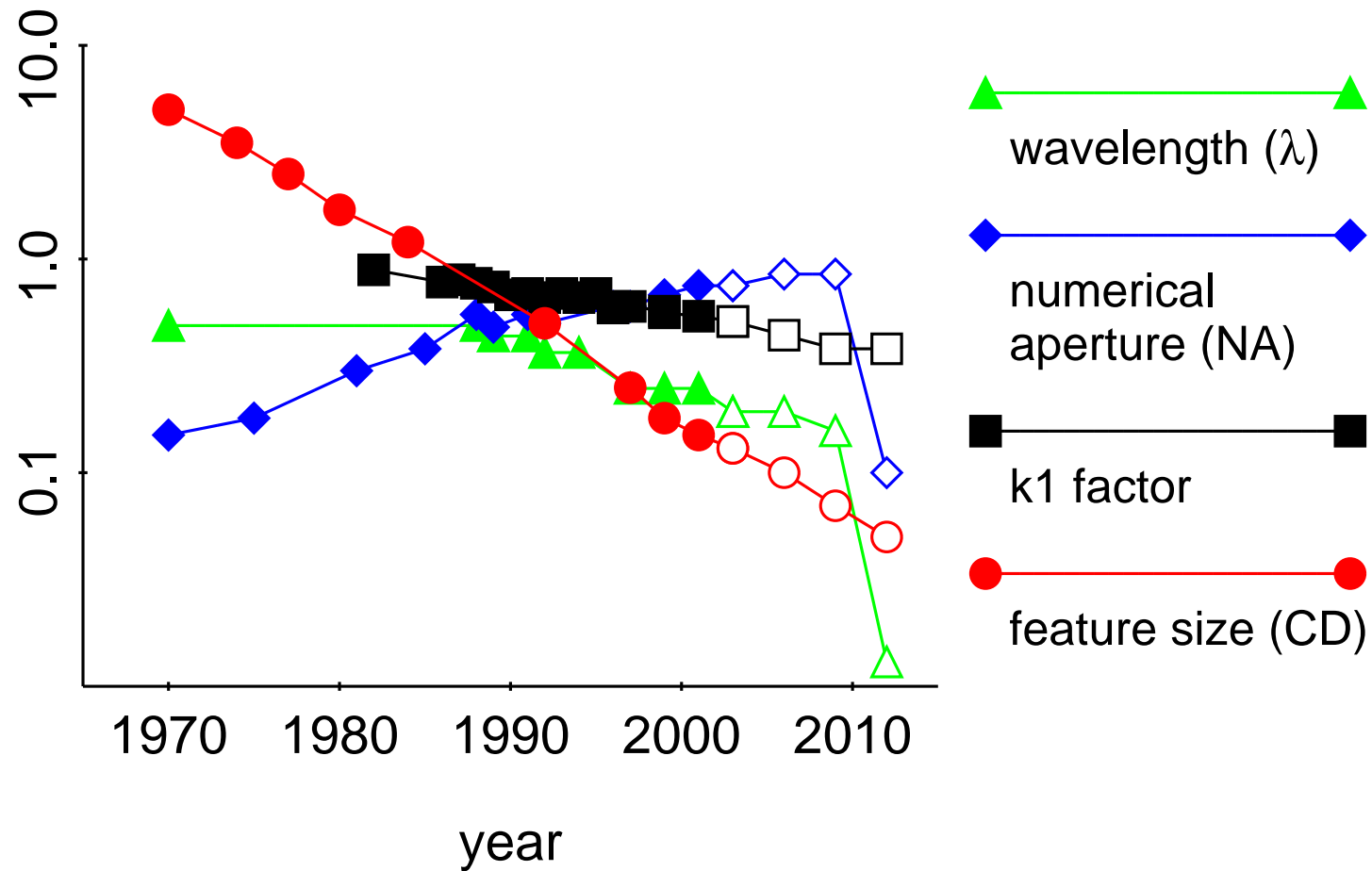


Cost per pixel



source: ASML

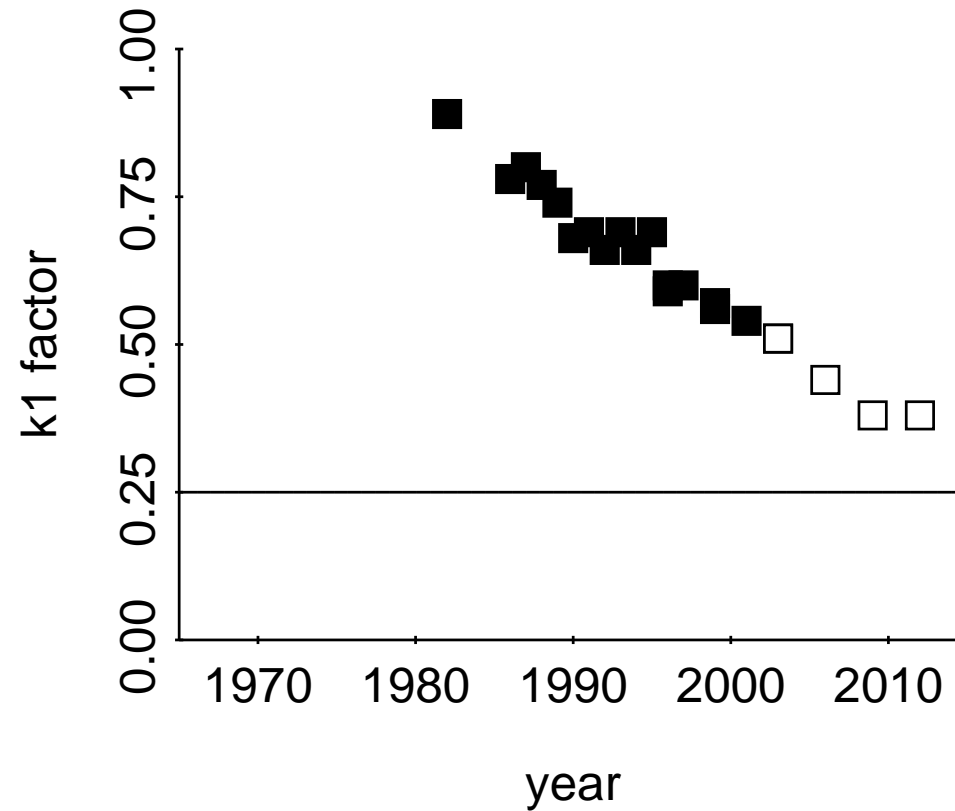
Evolution of various lithography parameters



$$CD = k_1 \times \frac{\lambda}{NA}$$

The k_1 factor

measure of lithography ease



traditional lithography: $k_1 \gtrapprox 0.75$

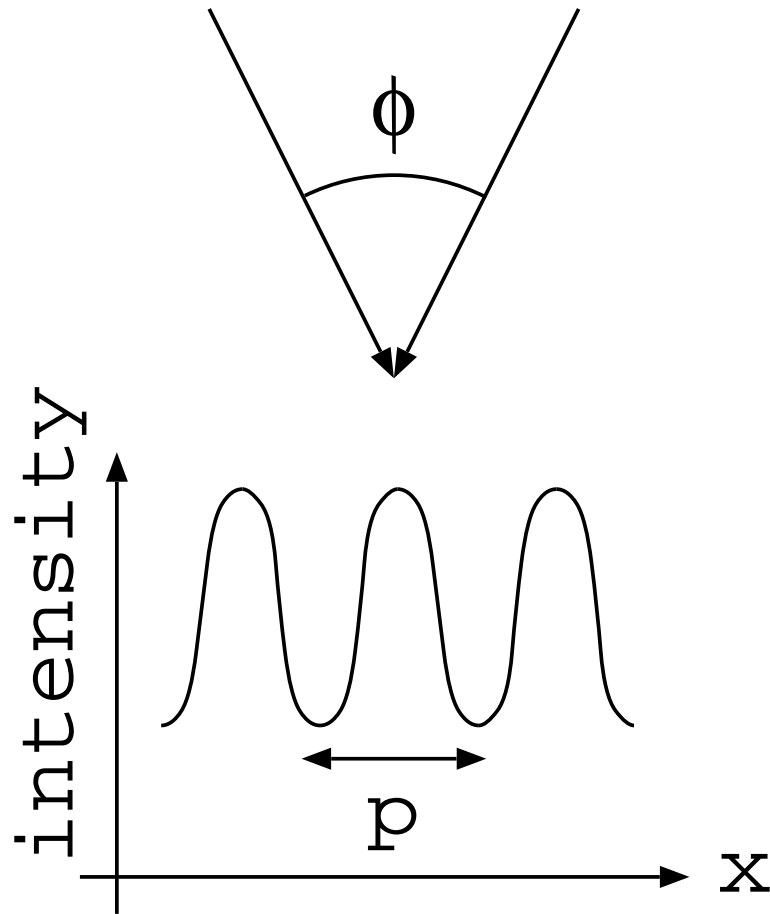
source: Bob Leidy at IBM

Outline

- Moore's law and microlithography
 - introduction
 - factors affecting resolution
 - trends
- low- k_1 challenges
 - resolution limit
 - image distortion and degradation
 - design and cost implications
- potential solutions

Image formed from two rays

circuit density limit (single exposure)

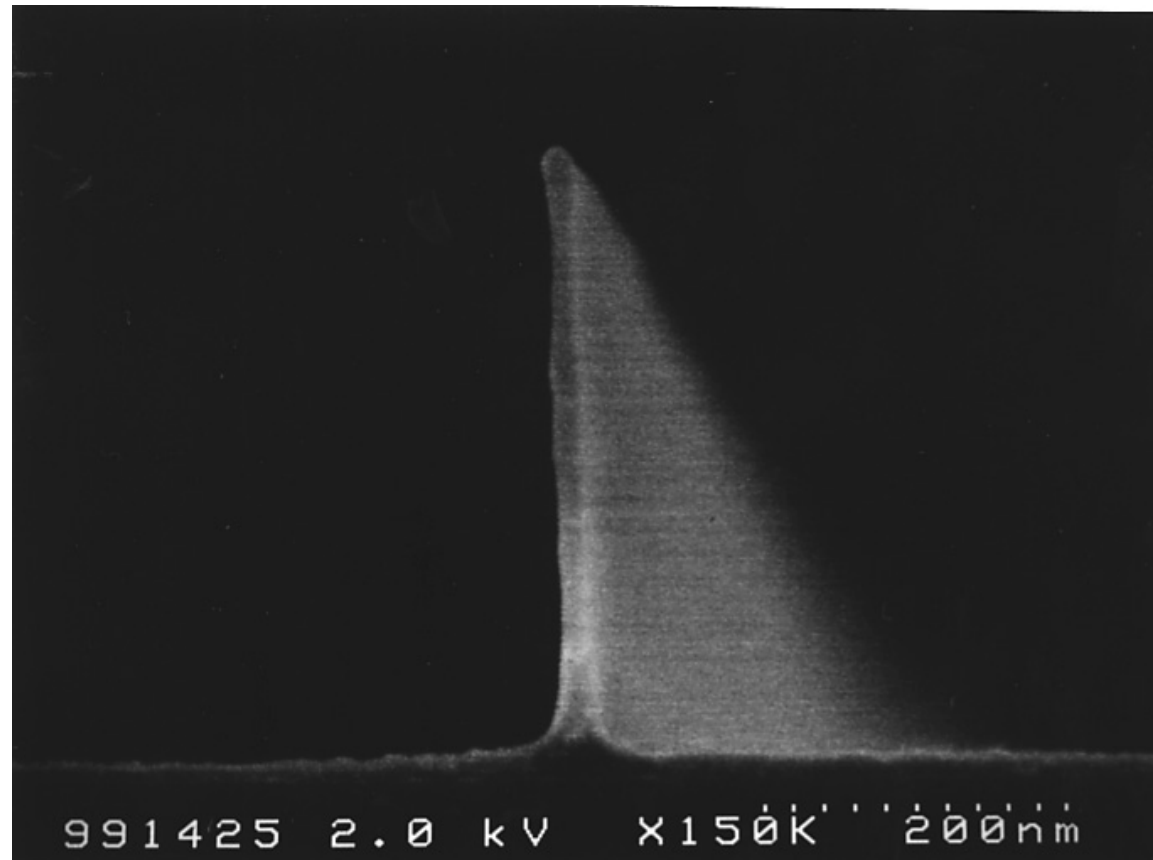


$$p = \frac{\lambda}{2 \sin \frac{\phi}{2}}$$
$$\sin \frac{\phi}{2} = |\sin \vartheta| \leq \sin \theta = \text{NA}$$

$$p_{\min} = \frac{\lambda}{2 \sin \theta}$$
$$= \frac{1}{2} \frac{\lambda}{\text{NA}}$$

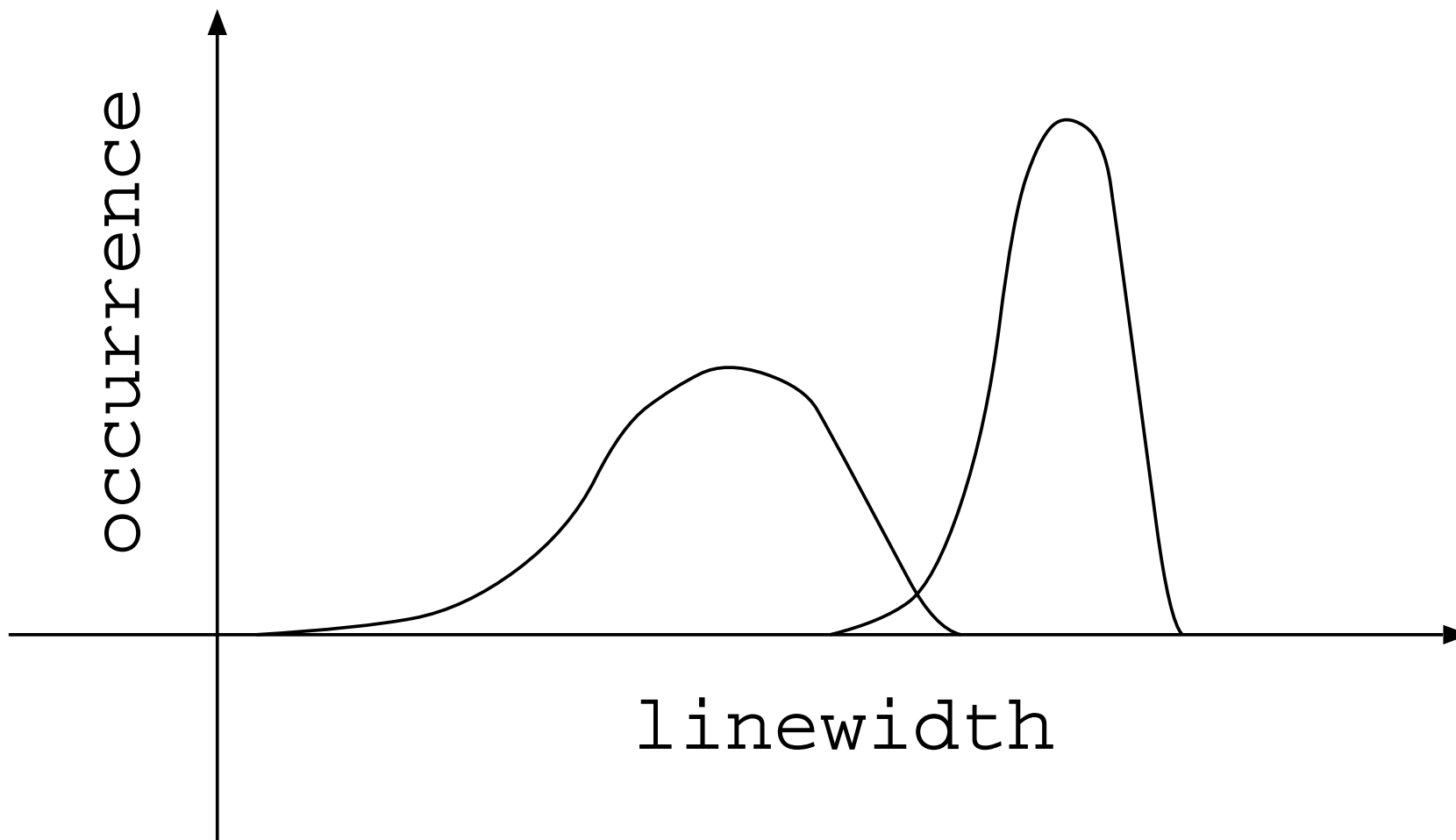
30-nm physical gate length

248-nm lithography



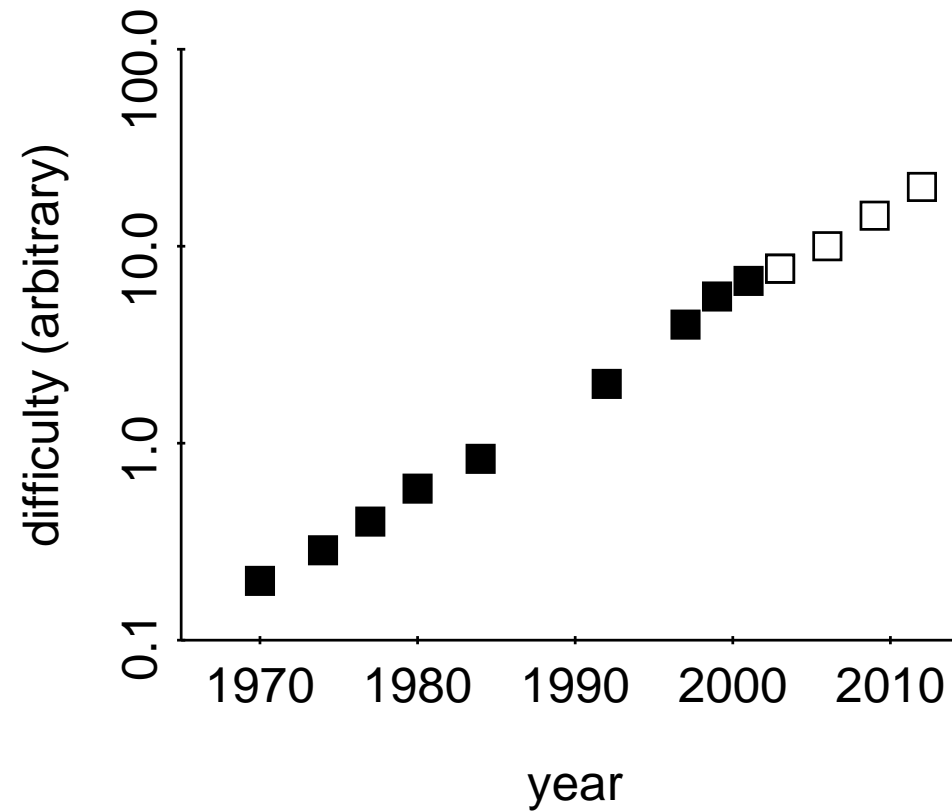
SEM courtesy of NAKAO Shuji at Mitsubishi

Resolution and linewidth control



Progress in microlithography

$$\text{difficulty} \propto \text{NA} \times (1/\lambda) \times (1/k_1)$$



Resolution limit

theoretical

$$p_{\min} = \frac{1}{2} \frac{\lambda}{\text{NA}}$$

$$\text{CD}_{\min} = \text{none}$$

practical (estimation)

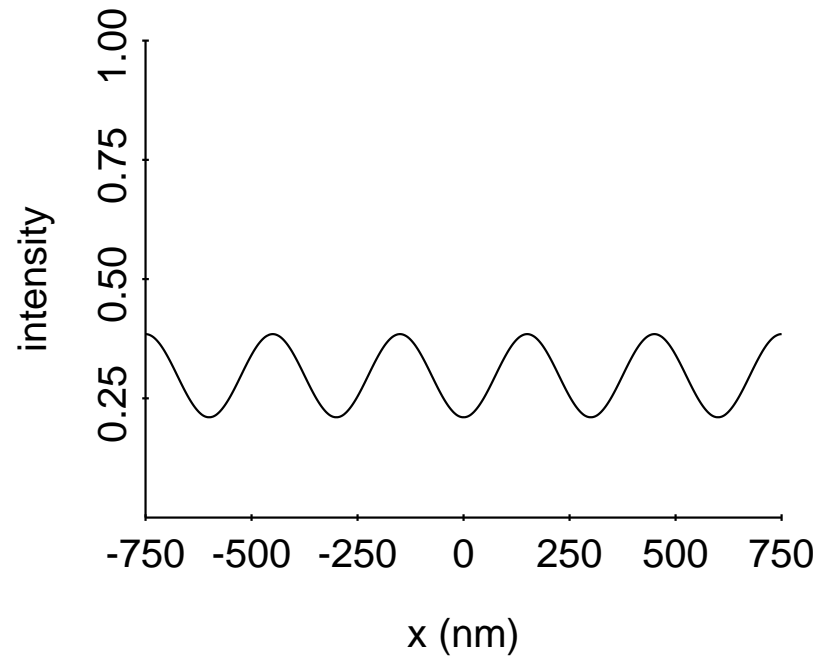
$$\begin{aligned} p_{\min} &\cong 0.7 \frac{\lambda}{\text{NA}} \\ &= 116 \text{ nm} \quad (\lambda = 157 \text{ nm}, \text{NA} = 0.95) \end{aligned}$$

$$\begin{aligned} \text{CD}_{\min} &\cong 0.2 \frac{\lambda}{\text{NA}} \\ &= 33 \text{ nm} \quad (\lambda = 157 \text{ nm}, \text{NA} = 0.95) \end{aligned}$$

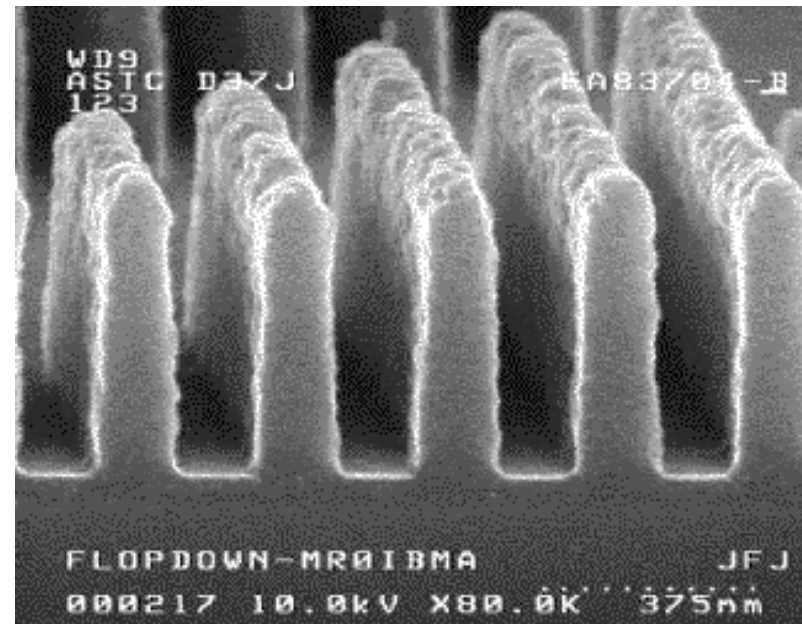
Some challenges of low- k_1 imaging

- image quality degradation (decreasing process latitude)
 - resolution enhancement techniques (phase-shifting masks, modified illumination, assist features)
- proximity effects
 - optical proximity correction (OPC)
- cost of ownership
- process latitude dependent on circuit patterns

The photoresist miracle



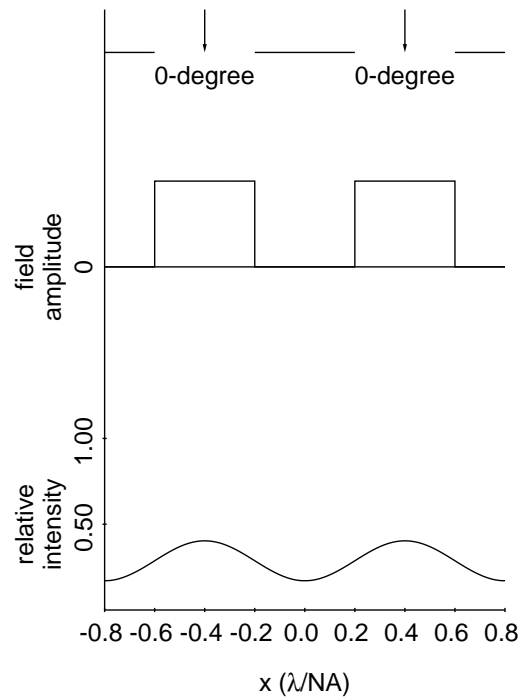
aerial image



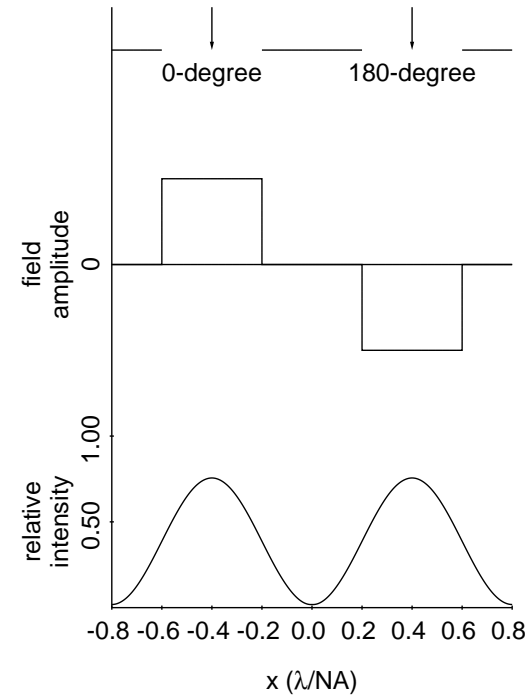
resist profile

Comparison between COG and alternating PSM

$0.4(\lambda/\text{NA})$ line

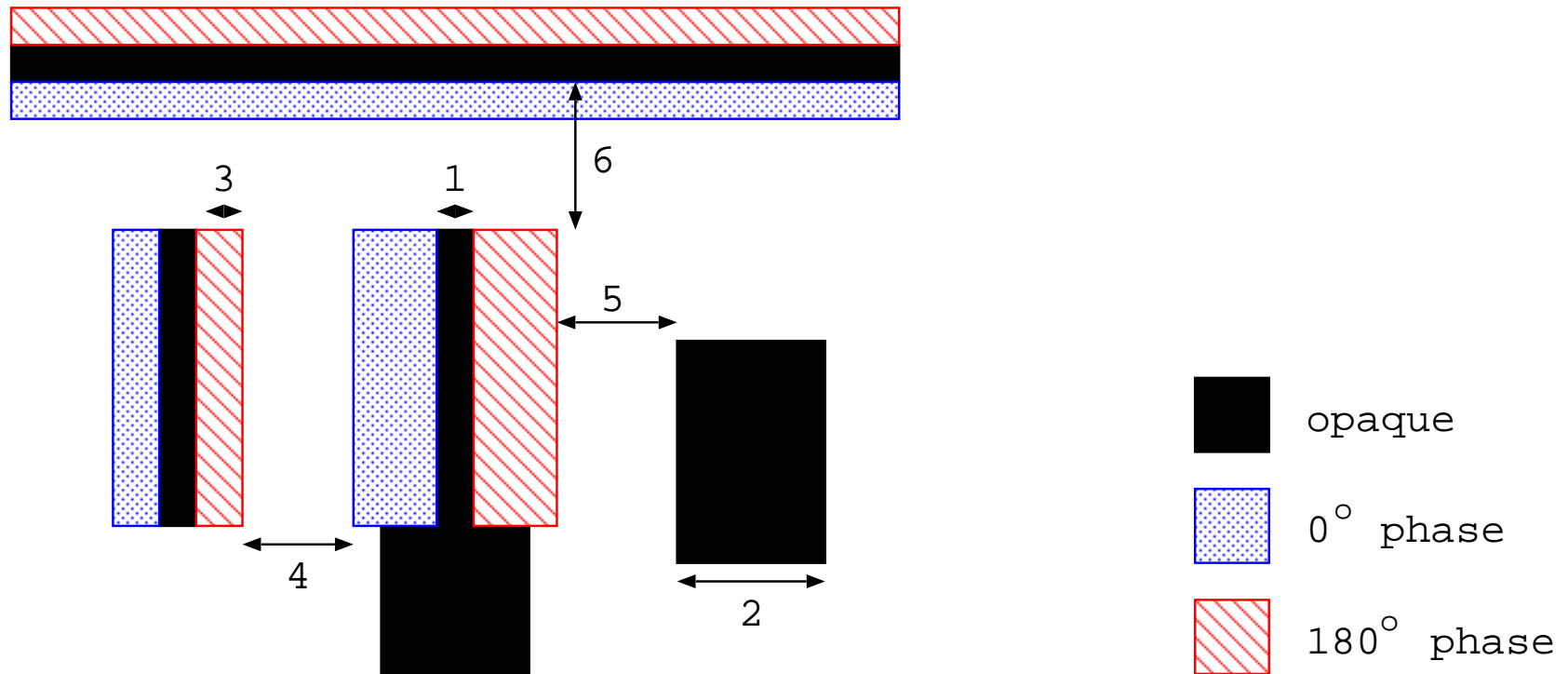


COG mask



alternating PSM

Typical circuit pattern



Design rules

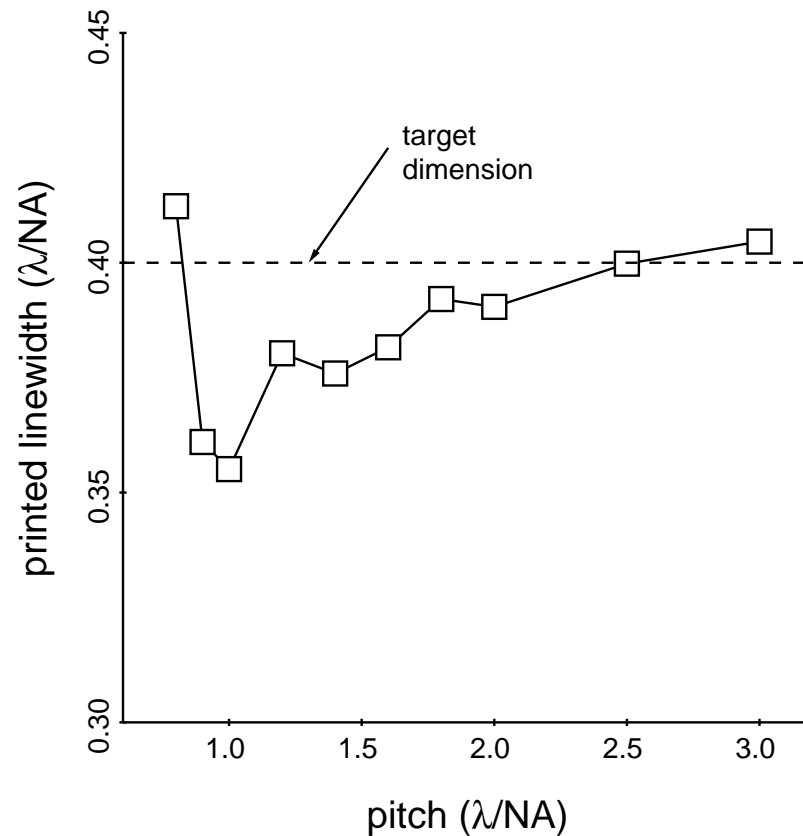
1. line sizes needing phase shifting,
 2. line size beyond which no phase shifting is needed,
 3. width of phase-shifting region,
 4. separation between phase-shifting regions,
 5. separation between phase-shifting and opaque regions,
 6. separation between critical line end to another critical line.
- may be more restrictive than traditional rules; possible tradeoff between density and CD
 - decision to use prior to process development

Some challenges of low- k_1 imaging

- image quality degradation (decreasing process latitude)
 - resolution enhancement techniques (phase-shifting masks, modified illumination, assist features)
- proximity effects
 - optical proximity correction (OPC)
- cost of ownership
- process latitude dependent on circuit patterns

Proximity effect

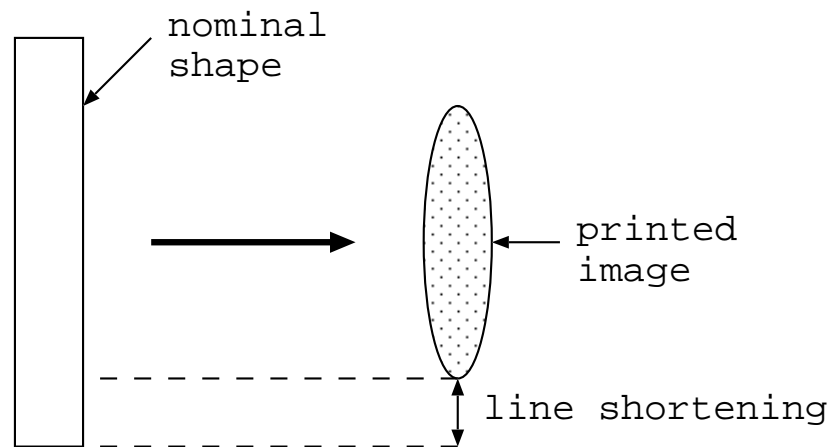
features with same nominal CD printing differently



- increases ACLV
- may cause nonprinting of critical features

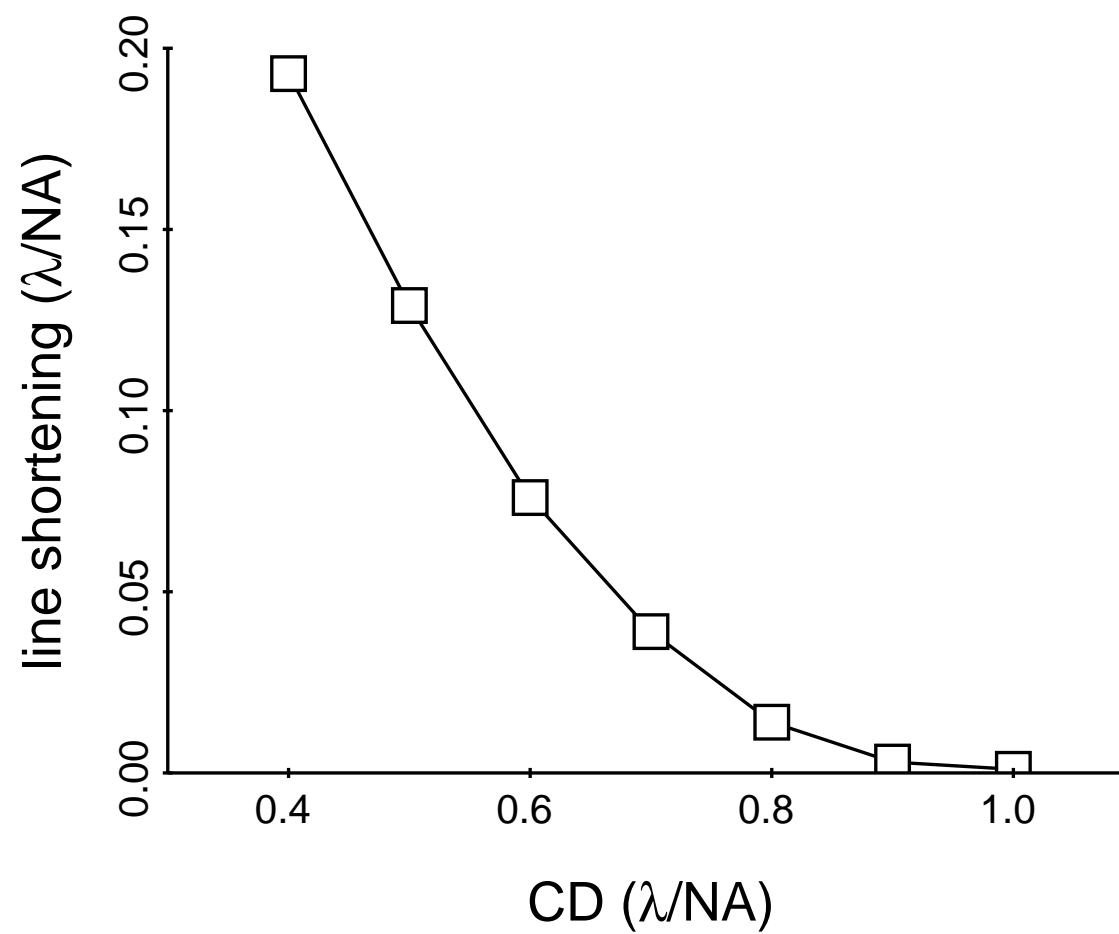
Line shortening

not foreshortening

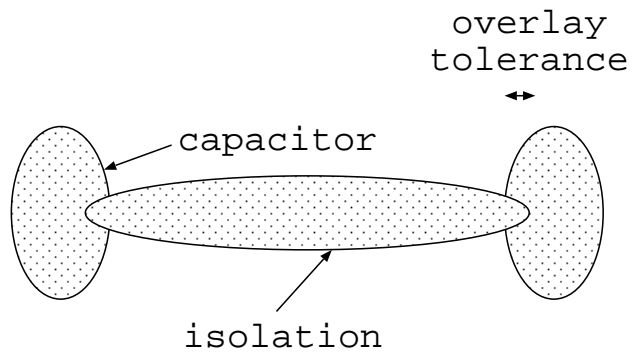
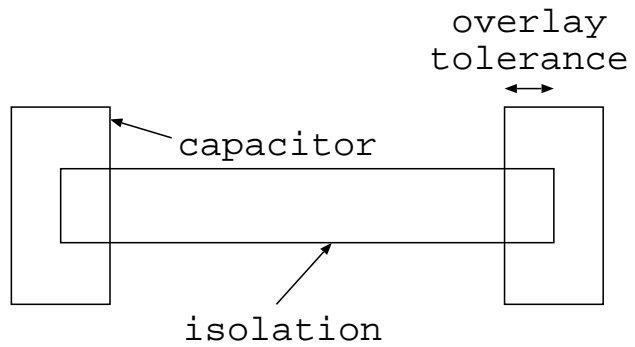


- diffraction
- mask rounding
- resist diffusion

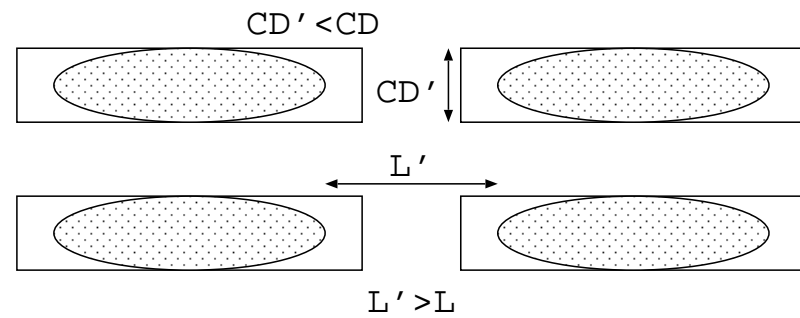
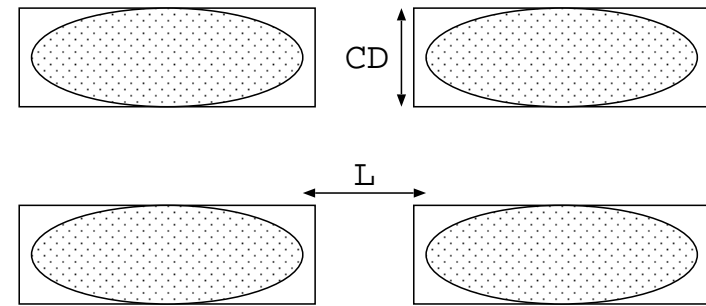
Line shortening worsens with decreasing k_1



Impact of line shortening

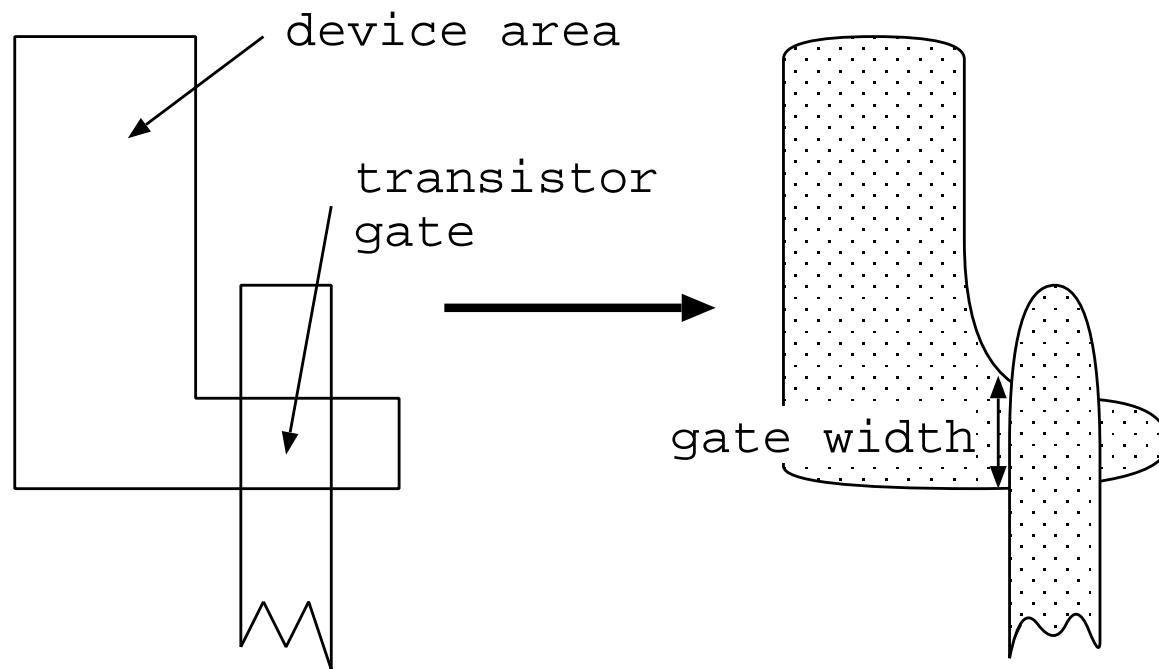


overlay control

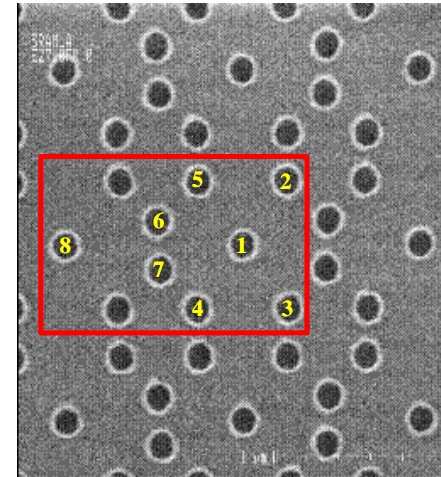
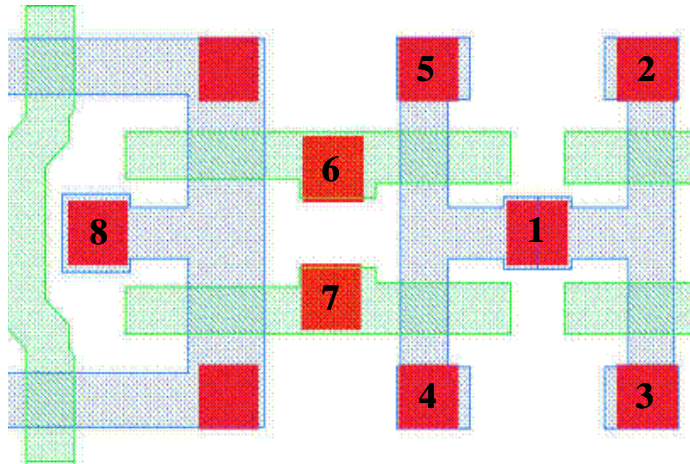


density impact

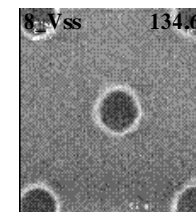
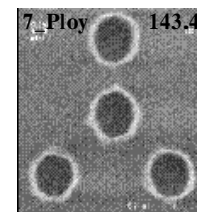
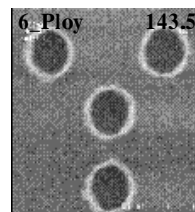
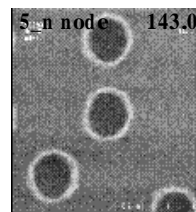
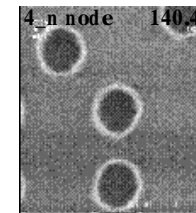
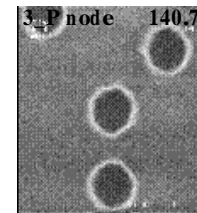
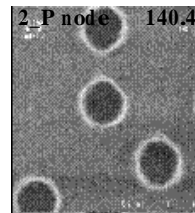
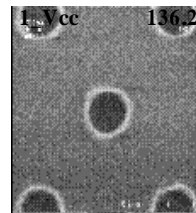
Corner rounding



CD variation caused by proximity



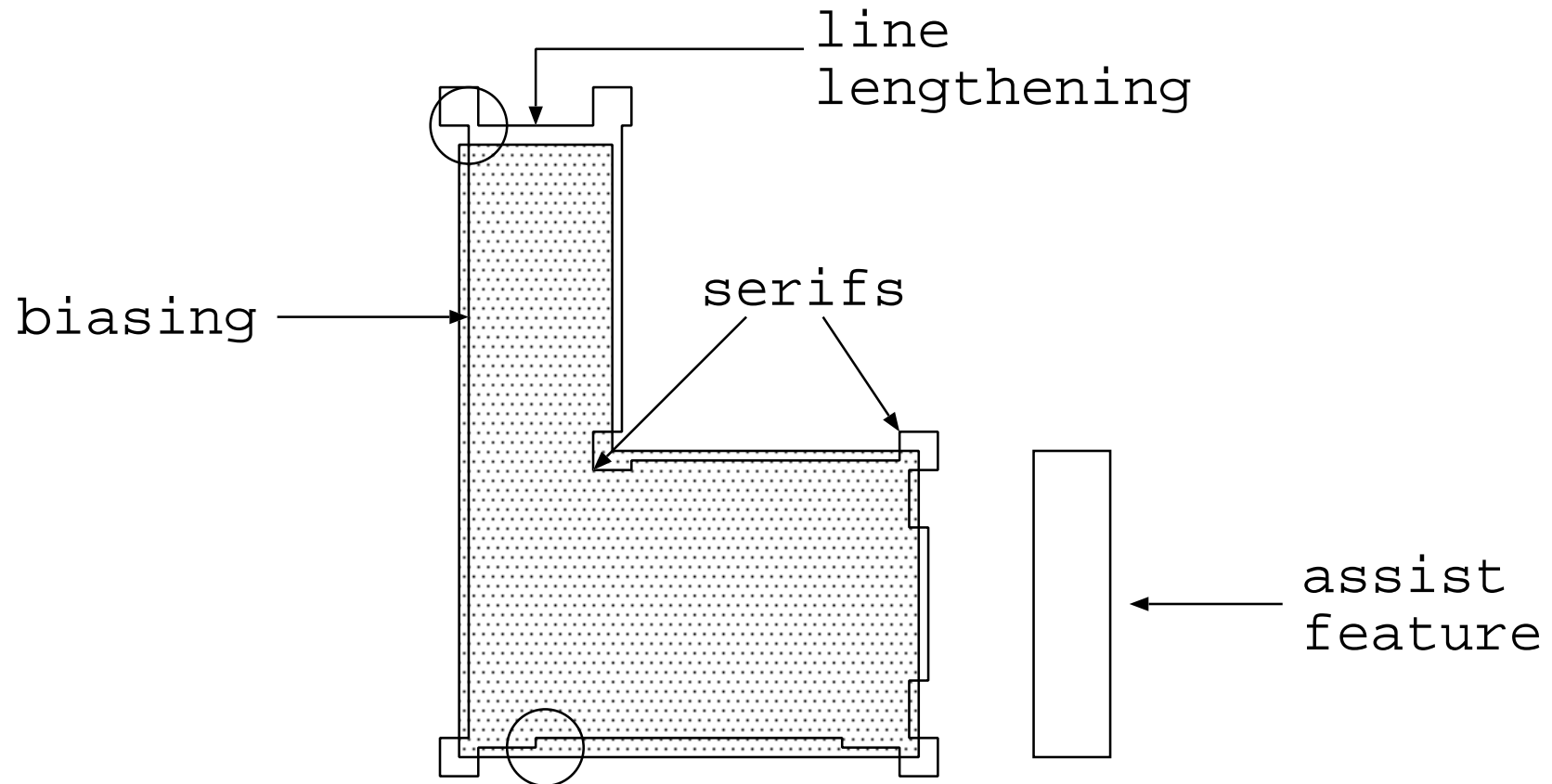
140-nm Contact Holes



source: TSMC

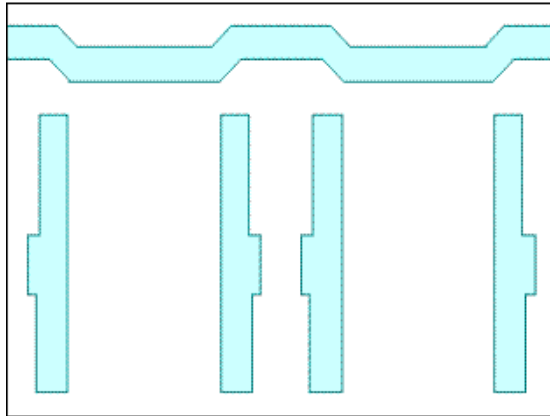
Optical proximity correction

typical predistortions

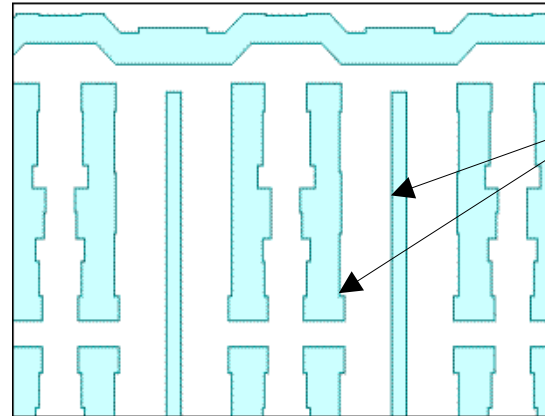


Optical proximity correction: an example

Original Layout (100 nm)

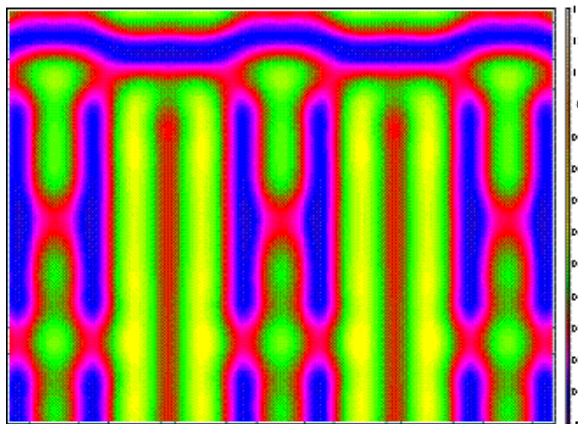


Post OPC Mask Pattern

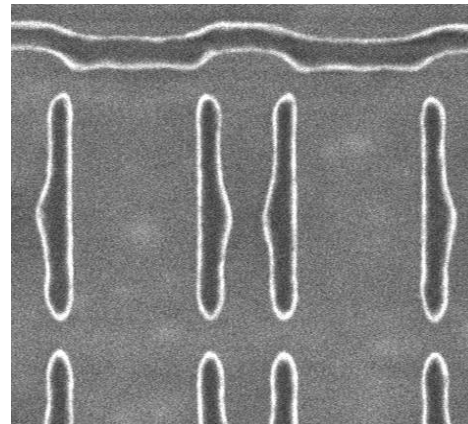


Model
based
OPC,
AF, and
attPSM for
enhanced
imaging

Intensity at Wafer Plane



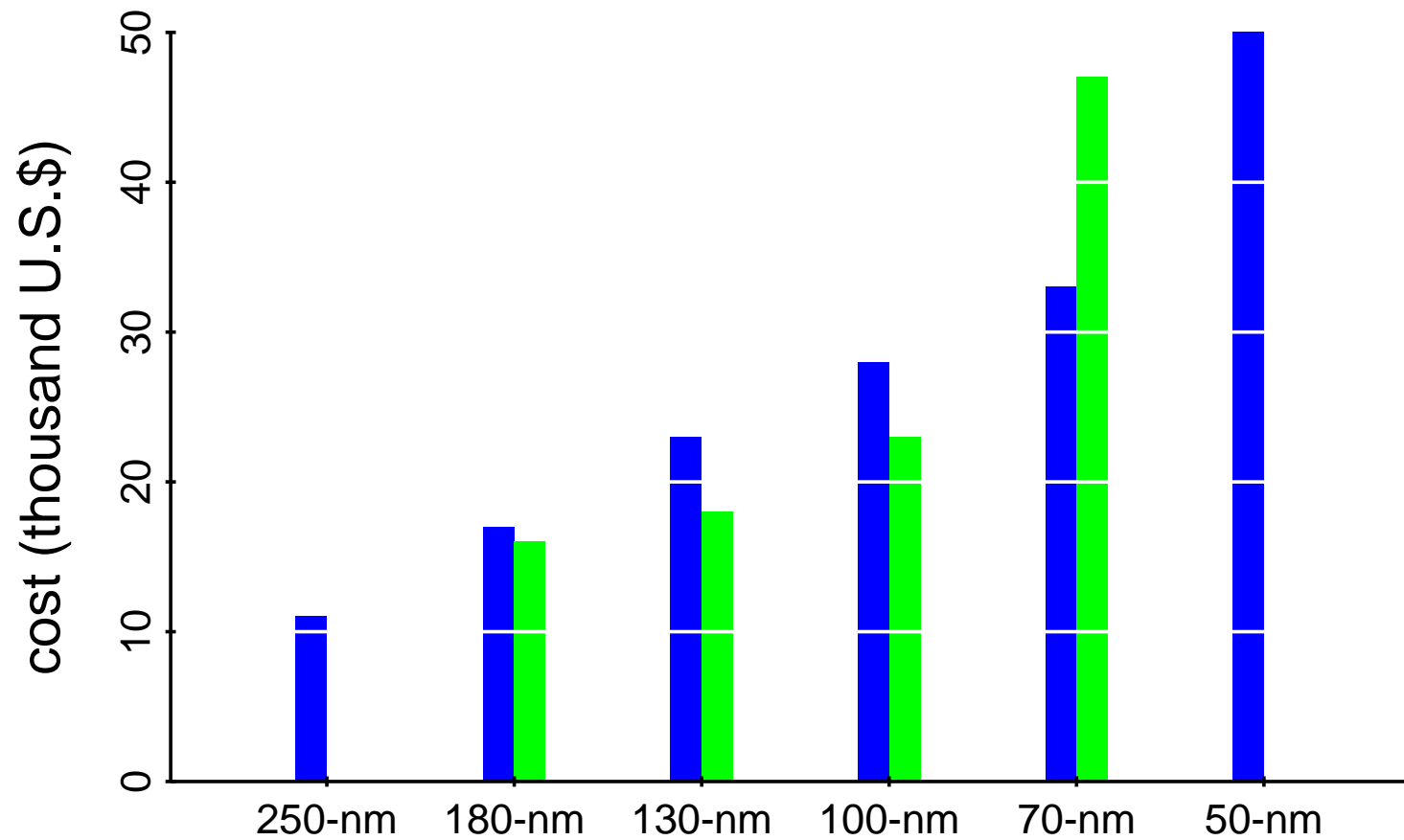
Pattern in Photoresist



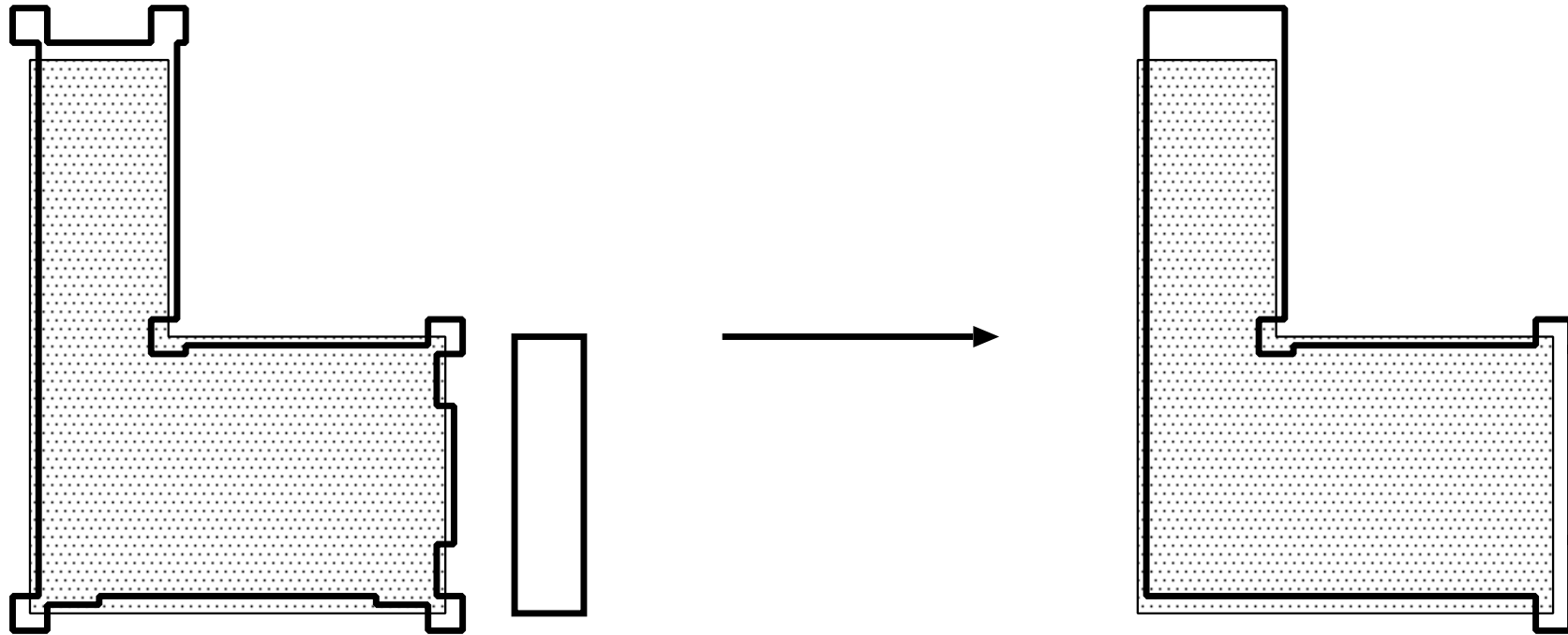
Imaged
with
0.63NA
193nm
scanner

Cost of reticles

1999 data



Frugal OPC

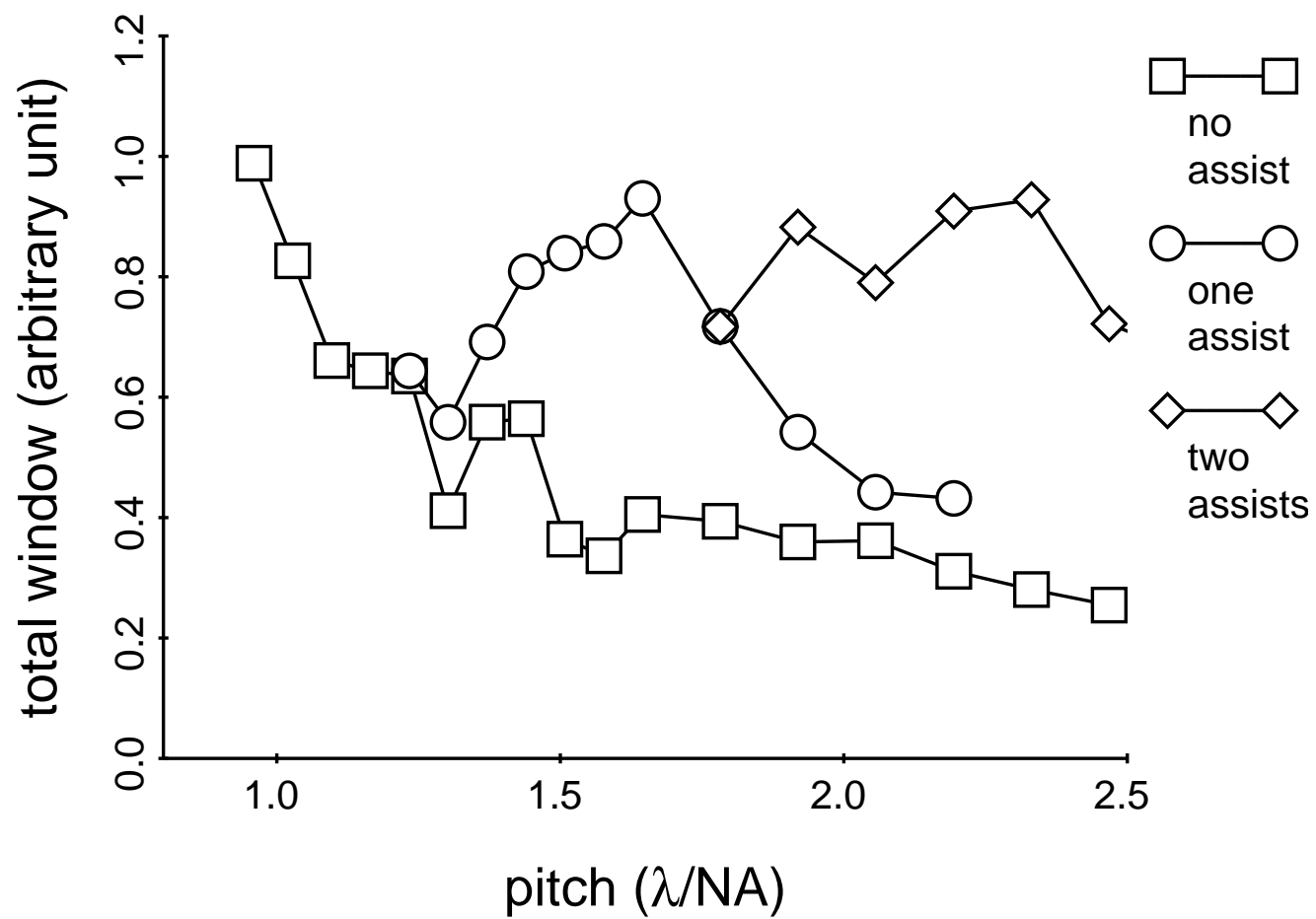


- need passing of functional information to OPC step
- would RETs impact higher-level steps such as synthesis?

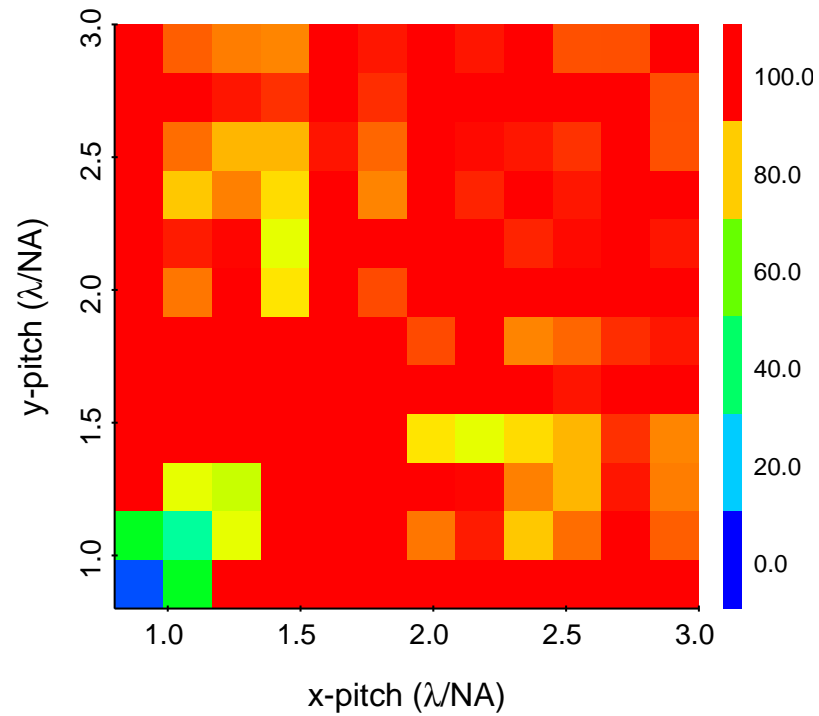
Some challenges of low- k_1 imaging

- image quality degradation (decreasing process latitude)
 - resolution enhancement techniques (phase-shifting masks, modified illumination, assist features)
- proximity effects
 - optical proximity correction (OPC)
- cost of ownership
- process latitude dependent on circuit patterns

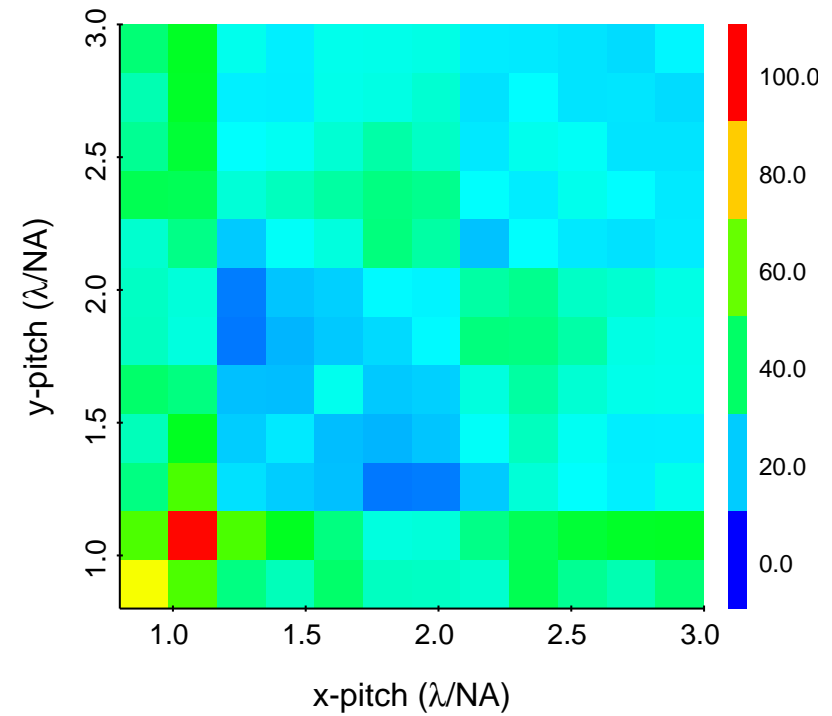
This line is not that line



The trouble with contacts

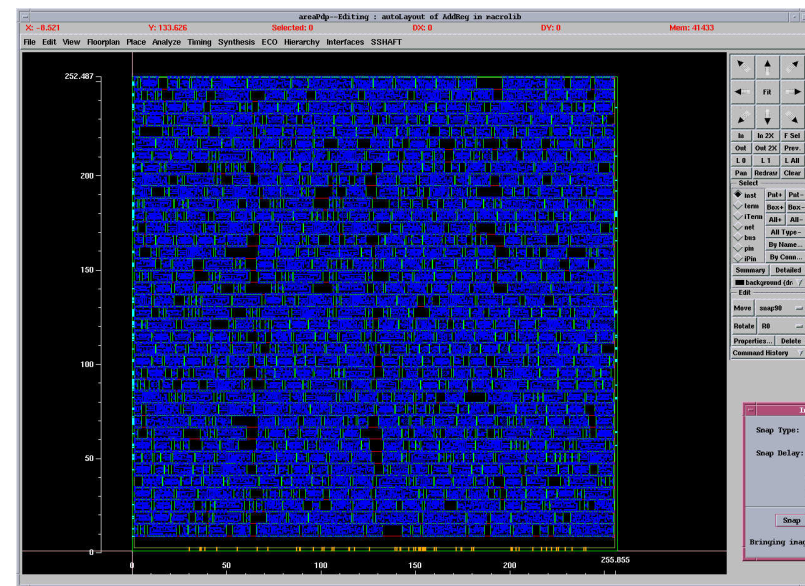
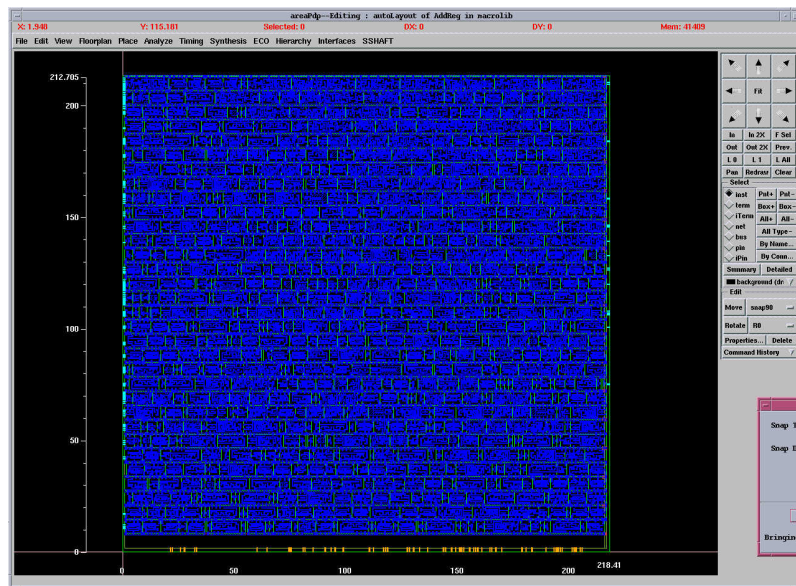


$\sigma = 0.45$



annular illumination

Impact of lithography-friendly design add-compare-select unit



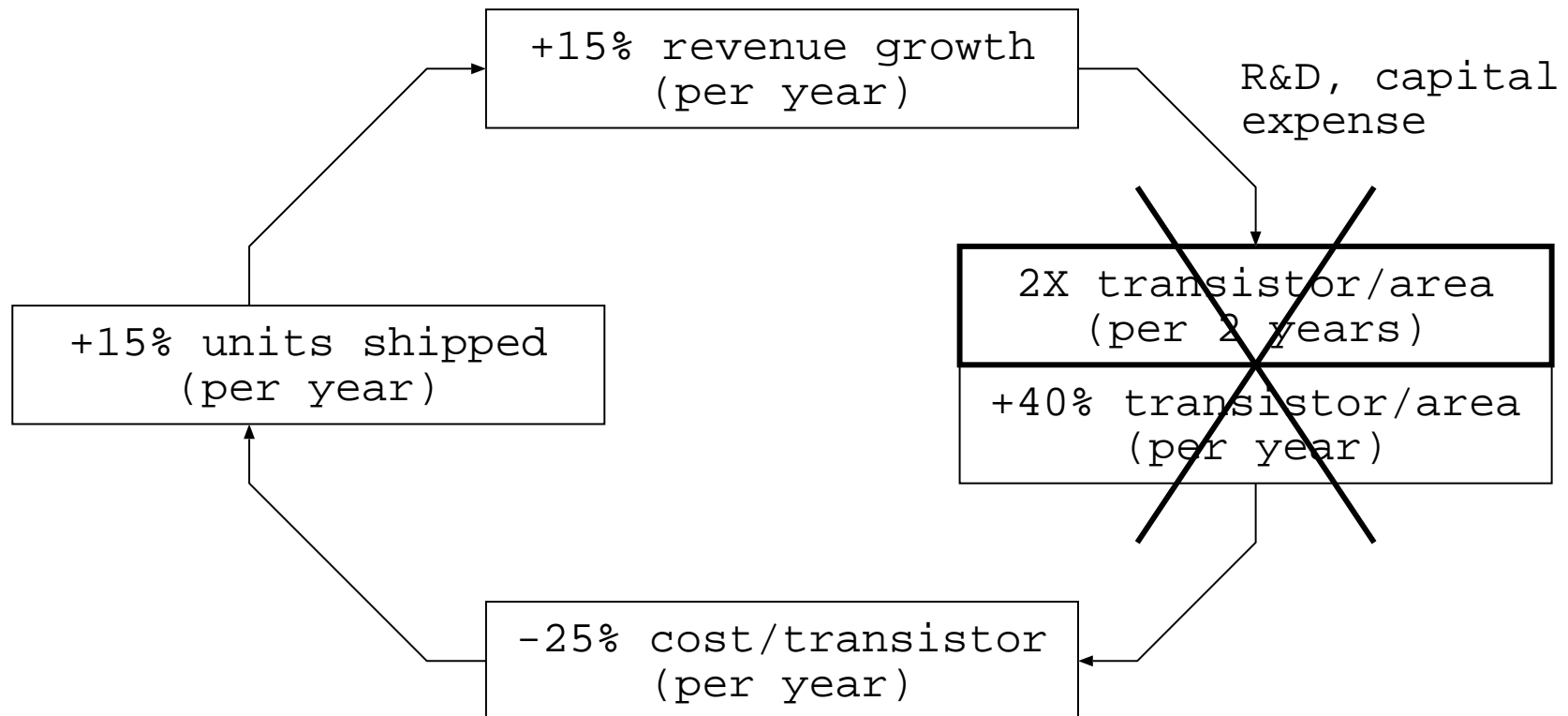
Outline

- Moore's law and microlithography
 - introduction
 - factors affecting resolution
 - trends
- low- k_1 challenges
 - resolution limit
 - image distortion and degradation
 - design and cost implications
- potential solutions

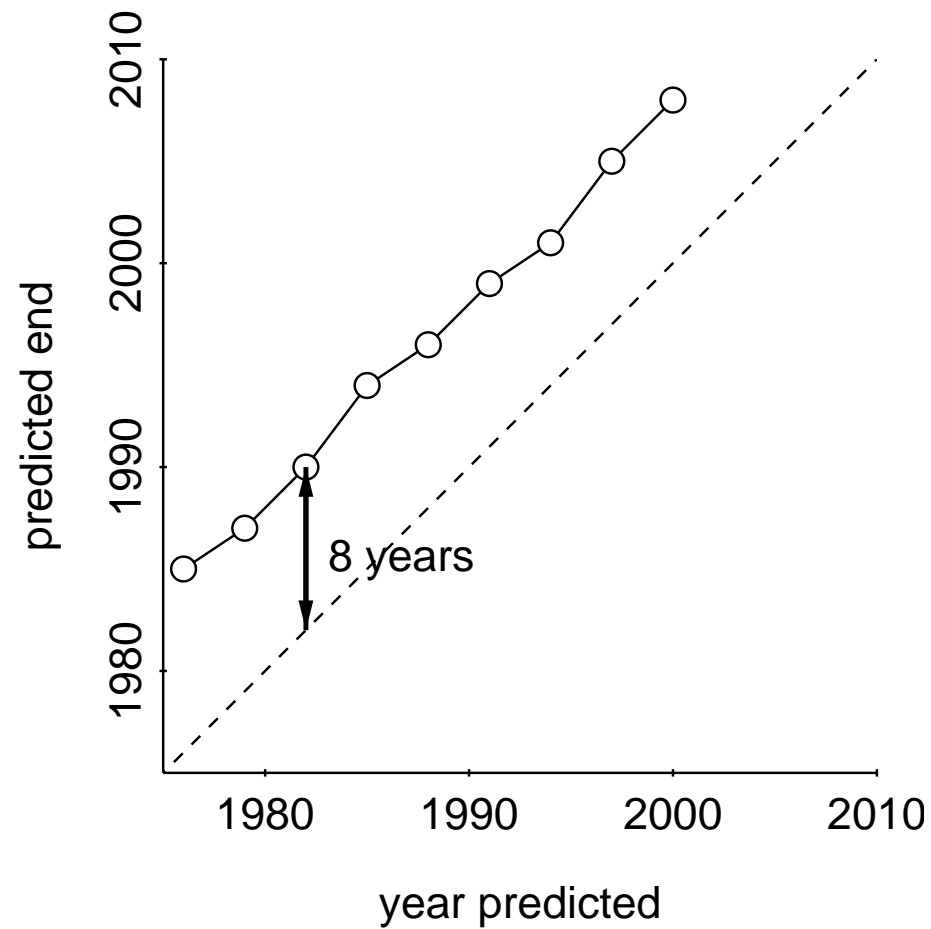
Summary

- optical lithography key to transistor miniaturization
- resolution approaching limit
 - ☐ wavelength (λ)
 - ☐ numerical aperture (NA)
 - ☐ k_1 factor
- challenges
 - ☐ image quality improvement
 - ☐ proximity effects
 - ☐ cost of ownership
- potential solutions
 - ☐ next-generation technology
 - ☐ improved design-fabrication interface

What if the semiconductor cycle breaks?



Predictions on end of optical lithography



source: John Sturtevant